TEXAS INSTRUMENTS
TLV9044-Q1
SBOSAK0 – JUNE 2024

# TLV904x-Q1 Automotive, 1.2V Ultra-Low Voltage, 10µA Micro-Power RRIO Amplifier for Power Conscious Applications

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, $T_A$
- Low power CMOS amplifier for cost-optimized applications
- Operational from supply voltage as low as 1.2V
- Low input bias current: 1pA typical, 12pA maximum
- Low quiescent current: 10µA/ch
- Low integrated noise of 6.5µ$V_{p-p}$ (0.1Hz to 10Hz)
- Rail-to-rail input and output
- High gain bandwidth product: 350kHz
- Thermal noise floor: 64nV/√Hz
- Low input offset voltage: ±0.6mV
- Unity-gain stable
- Robust drive of 100pF of load capacitance
- Internal RFI and EMI filtered input pins

## 2 Applications

- HEV/EV OBC & DC/DC converter
- Kick to open module
- Thermal management
- Car access & security systems

## 3 Description

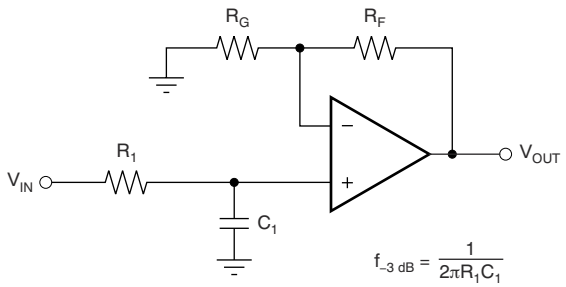
The low-power TLV904x-Q1 family includes single, dual, and quad-channel ultra-low-voltage (1.2V to 5.5V) operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. The TLV904x-Q1 enables power savings both with the low quiescent current (10µA, typical) and the ability to operate at supply voltages as low as 1.2V. These devices are designed to be cost-effective for power and space-constrained applications where low-voltage operation is crucial.

The robust design of the TLV904x-Q1 family simplifies circuit design. These op amps feature an integrated RFI and EMI rejection filter, unity-gain stability, and no-phase reversal in input overdrive conditions. The device also delivers excellent AC performance with a gain bandwidth of 350kHz and a high capacitive load drive of 100pF, enabling designers to achieve both improved performance and lower power consumption.

**Device Information**

| PART NUMBER(1) | CHANNEL COUNT | PACKAGE | PACKAGE SIZE (4) |
|---|---|---|---|
| TLV9041-Q1(2) | Single | DBV (SOT-23, 5) | 2.9mm × 2.80mm |
| | | DCK (SC70, 5) | 2.00mm × 2.10mm |
| TLV9042-Q1(2) | Dual | D (SOIC, 8) | 4.90mm × 6.00mm |
| | | DGK (VSSOP, 8) | 3.00mm × 4.90mm |
| | | PW (TSSOP, 8) | 3.00mm × 6.40mm |
| TLV9044-Q1 | Quad | D (SOIC, 14)(3) | 8.65mm × 6.00mm |
| | | PW (TSSOP, 14) | 5.00mm × 6.40mm |
| | | DYY (SOT-23, 14) (3) | 4.20mm × 3.26mm |

(1) For all available packages, see the orderable addendum in Section 10.
(2) This device is for preview only.
(3) This package is for preview only.
(4) The package size (length x width) is a nominal value and includes pins, where applicable..




**Single-Pole, Low-Pass Filter**

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## 4 Pin Configuration and Functions

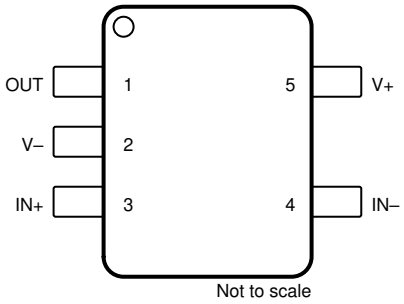


**Figure 4-1. TLV9041-Q1 DBV Package: 5-Pin SOT-23[1] Top View**

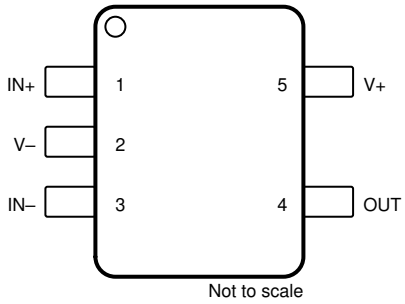


**Figure 4-2. TLV9041-Q1 DCK Package: 5-Pin SC70[1] Top View**

**Table 4-1. Pin Functions: TLV9041-Q1**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOT-23 | SC70 | | |
| IN– | 4 | 3 | I | Inverting input |
| IN+ | 3 | 1 | I | Noninverting input |
| OUT | 1 | 4 | O | Output |
| V– | 2 | 2 | I or — | Negative (low) supply or ground (for single-supply operation) |
| V+ | 5 | 5 | I | Positive (high) supply |

(1) This package is preview only.

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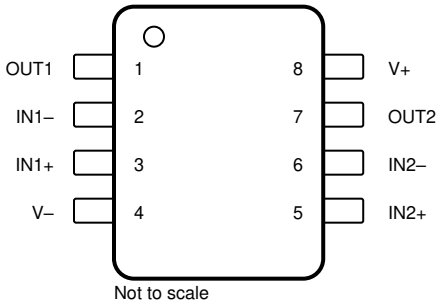


**Figure 4-3. TLV9042-Q1 D, PW, and DGK Packages: 8-Pin SOIC, TSSOP, and VSSOP(1) Top View**

**Table 4-2. Pin Functions: TLV9042-Q1**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN1– | 2 | I | Inverting input, channel 1 |
| IN1+ | 3 | I | Noninverting input, channel 1 |
| IN2– | 6 | I | Inverting input, channel 2 |
| IN2+ | 5 | I | Noninverting input, channel 2 |
| OUT1 | 1 | O | Output, channel 1 |
| OUT2 | 7 | O | Output, channel 2 |
| V– | 4 | I | Negative (low) supply or ground (for single-supply operation) |
| V+ | 8 | I | Positive (high) supply |

(1) These packages are preview only.

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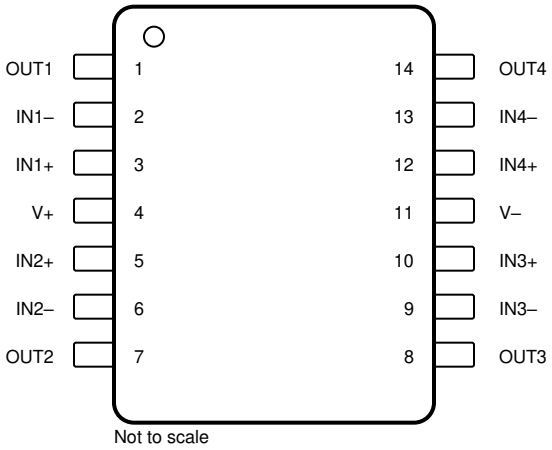


**Figure 4-4. TLV9044-Q1 D, PW and DYY Packages: 14-Pin SOIC, TSSOP and SOT-23(1) Top View**

**Table 4-3. Pin Functions: TLV9044-Q1**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN1– | 2 | I | Inverting input, channel 1 |
| IN1+ | 3 | I | Noninverting input, channel 1 |
| IN2– | 6 | I | Inverting input, channel 2 |
| IN2+ | 5 | I | Noninverting input, channel 2 |
| IN3– | 9 | I | Inverting input, channel 3 |
| IN3+ | 10 | I | Noninverting input, channel 3 |
| IN4– | 13 | I | Inverting input, channel 4 |
| IN4+ | 12 | I | Noninverting input, channel 4 |
| NC | — | — | No internal connection |
| OUT1 | 1 | O | Output, channel 1 |
| OUT2 | 7 | O | Output, channel 2 |
| OUT3 | 8 | O | Output, channel 3 |
| OUT4 | 14 | O | Output, channel 4 |
| V– | 11 | I or — | Negative (low) supply or ground (for single-supply operation) |
| V+ | 4 | I | Positive (high) supply |

(1) D (SOIC) and DYY (SOT-23) packages are preview only.

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_S$ = (V+) – (V–) | | 0 | 6.0 | V |
| Signal input pins | Common-mode voltage (2) | (V–) – 0.5 | (V+) + 0.5 | V |
| | Differential voltage (2) | | $V_S$ + 0.2 | V |
| | Current (2) | –10 | 10 | mA |
| Output short-circuit (3) | | Continuous | | |
| Operating ambient temperature, $T_A$ | | –55 | 150 | °C |
| Junction temperature, $T_J$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC-Q100-002 (1) | ±3000 | V |
| | | Charged-device model (CDM), per AEC-Q100-001 | ±1500 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Supply voltage, (V+) – (V–) | 1.2 | 5.5 | V |
| $V_I$ | Input voltage range | (V–) | (V+) | V |
| $T_A$ | Specified temperature | –40 | 125 | °C |

## 5.4 Thermal Information for Quad Channel

| THERMAL METRIC (1) | | TLV9044-Q1 | | | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) | PW (TSSOP) | DYY (SOT-23-14) | |
| | | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | TBD | TBD | TBD | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | TBD | TBD | TBD | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | TBD | TBD | TBD | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | TBD | TBD | TBD | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | TBD | TBD | TBD | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

## 5.5 Electrical Characteristics

For $V_S$ = (V+) – (V–) = 1.2V to 5.5V (±0.6V to ±2.75V) at $T_A$ = 25°C, $R_L$ = 100kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{O\ UT}$ = $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | | | | ±0.6 | ±2.25 | mV |
| | | | $T_A$ = –40°C to 125°C | | | ±2.5 | |
| $dV_{OS}/dT$ | Input offset voltage drift | | $T_A$ = –40°C to 125°C | | ±0.8 | | µV/°C |
| PSRR | Input offset voltage versus power supply | $V_S$ = ±0.6V to ±2.75V , $V_{CM}$ = V– | | | ±20 | ±100 | µV/V |
| | Channel separation | f = 10kHz | | | ±5.6 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current (1) | | | | ±1 | ±12 | pA |
| $I_{OS}$ | Input offset current (1) | | | | ±0.5 | ±10 | pA |
| **NOISE** | | | | | | | |
| $E_N$ | Input voltage noise | f = 0.1Hz to 10Hz | | | 6.5 | | $\mu V_{PP}$ |
| $e_N$ | Input voltage noise density | f = 100Hz | | | 85 | | nV/√Hz |
| | | f = 1kHz | | | 66 | | |
| | | f = 10kHz | | | 64 | | |
| $i_N$ | Input current noise (2) | f = 1kHz | | | 20 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | |
| $V_{CM}$ | Common-mode voltage range | | | (V–) | | (V+) | V |
| CMRR | Common-mode rejection ratio | (V–) < $V_{CM}$ < (V+) – 0.7V, $V_S$ = 1.2V | $T_A$ = –40°C to 125°C | 60 | 77 | | dB |
| | | (V–) < $V_{CM}$ < (V+) – 0.7V, $V_S$ = 5.5V | | 75 | 89 | | |
| | | (V–) < $V_{CM}$ < (V+), $V_S$ = 1.2V | | | 60 | | |
| | | (V–) < $V_{CM}$ < (V+), $V_S$ = 5.5V | | 57 | 72 | | |
| **INPUT IMPEDANCE** | | | | | | | |
| $Z_{ID}$ | Differential | | | | 80 \|\| 1.4 | | GΩ \|\| pF |
| $Z_{ICM}$ | Common-mode | | | | 100 \|\| 0.5 | | GΩ \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $V_S$ = 1.2V, (V–) + 0.2V < $V_O$ < (V+) – 0.2V, $R_L$ = 10kΩ to $V_S$ / 2 | $T_A$ = –40°C to 125°C | | 98 | | dB |
| | | $V_S$ = 5.5V, (V–) + 0.2V < $V_O$ < (V+) – 0.2V, $R_L$ = 10kΩ to $V_S$ / 2 | | | 125 | | |
| | | $V_S$ = 1.2V, (V–) + 0.1V < $V_O$ < (V+) – 0.1V, $R_L$ = 100kΩ to $V_S$ / 2 | | | 105 | | |
| | | $V_S$ = 5.5V, (V–) + 0.1V < $V_O$ < (V+) – 0.1V, $R_L$ = 100kΩ to $V_S$ / 2 | | 107 | 130 | | |
| **FREQUENCY RESPONSE** | | | | | | | |
| THD+N | Total harmonic distortion + noise (3) | $V_S$ = 5.5V, $V_{CM}$ = 2.75V, $V_O$ = 1$V_{RMS}$, G = +1, f = 1kHz, $R_L$ = 100kΩ to $V_S$ / 2 | | | 0.013 | | % |
| GBW | Gain-bandwidth product | $R_L$ = 1MΩ connected to $V_S$/2 | | | 350 | | kHz |
| SR | Slew rate | $V_S$ = 5.5V, G = +1, $C_L$ = 10pF | | | 0.2 | | V/µs |
| $t_S$ | Settling time | To 0.1%, $V_S$ = 5.5V, $V_{STEP}$ = 4V, G = +1, $C_L$ = 10pF | | | 25 | | µs |
| | | To 0.1%, $V_S$ = 5.5V, $V_{STEP}$ = 2V, G = +1, $C_L$ = 10pF | | | 22 | | |
| | | To 0.01%, $V_S$ = 5.5V, $V_{STEP}$ = 4V, G = +1, $C_L$ = 10pF | | | 35 | | |
| | | To 0.01%, $V_S$ = 5.5V, $V_{STEP}$ = 2V, G = +1, $C_L$ = 10pF | | | 30 | | |
| | Phase margin | G = +1, $R_L$ = 100kΩ connected to $V_S$/2, $C_L$ = 10pF | | | 65 | | ° |
| | Overload recovery time | $V_{IN}$ × gain > $V_S$ | | | 13 | | µs |
| EMIRR | Electro-magnetic interference rejection ratio | f = 1GHz, $V_{IN\_EMIRR}$ = 100mV | | | 70 | | dB |

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For $V_S$ = (V+) – (V–) = 1.2V to 5.5V (±0.6V to ±2.75V) at $T_A$ = 25°C, $R_L$ = 100kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{O\ UT}$ = $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | | |
| | Voltage output swing from rail | Positive rail headroom | $V_S$ = 1.2V, $R_L$ = 100kΩ to $V_S$ / 2 | | 0.75 | 7 | mV |
| | | | $V_S$ = 5.5V, $R_L$ = 10kΩ to $V_S$ / 2 | | 10 | 21 | |
| | | | $V_S$ = 5.5V, $R_L$ = 100kΩ to $V_S$ / 2 | | 1 | 8 | |
| | | Negative rail headroom | $V_S$ = 1.2V, $R_L$ = 100kΩ to $V_S$ / 2 | | 0.75 | 5 | |
| | | | $V_S$ = 5.5V, $R_L$ = 10kΩ to $V_S$ / 2 | | 10 | 21 | |
| | | | $V_S$ = 5.5V, $R_L$ = 100kΩ to $V_S$ / 2 | | 1 | 8 | |
| $I_{SC}$ | Short-circuit current (4) | $V_S$ = 5.5V | | | ±40 | | mA |
| $Z_O$ | Open-loop output impedance | f = 10kHz | | | 7500 | | Ω |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | $V_S$ = 5.5V, $I_O$ = 0A | | | 10 | 13 | µA |
| | | | $T_A$ = –40°C to 125°C | | | 13.5 | |
| **SHUTDOWN** | | | | | | | |

(1) Maximum $I_B$ and $I_{OS}$ limits are specified based on characterization results. Input differential voltages greater than 2.5V can cause increased $I_B$
(2) Typical input current noise data is specified based on design simulation results
(3) Third-order filter; bandwidth = 80kHz at –3dB.
(4) Short-circuit current is average of sourcing and sinking short circuit currents

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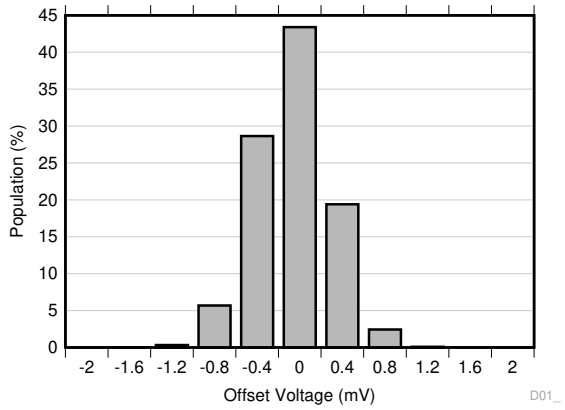
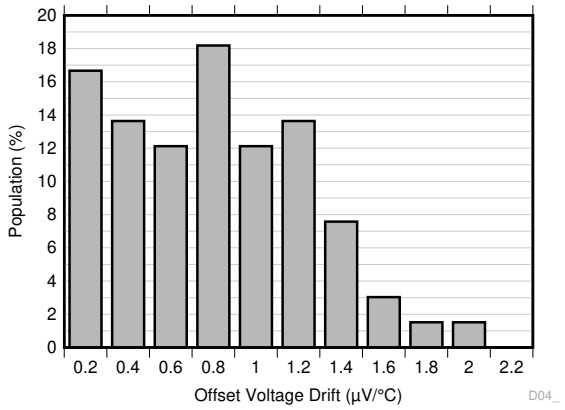
## 5.6 Typical Characteristics

at $T_A$ = 25°C, V+ = 2.75V, V– = –2.75V, $R_L$ = 10kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)



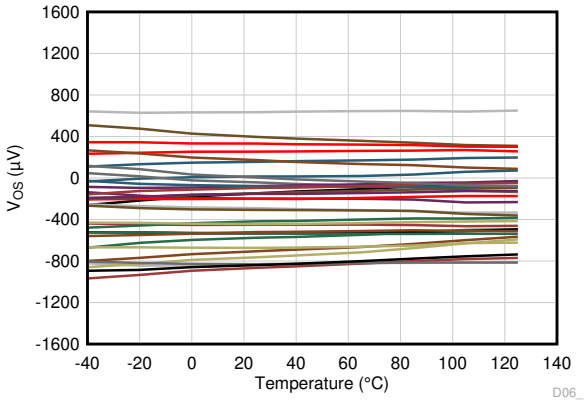

$V_S$ = 5.5V

**Figure 5-1. Offset Voltage Distribution Histogram**



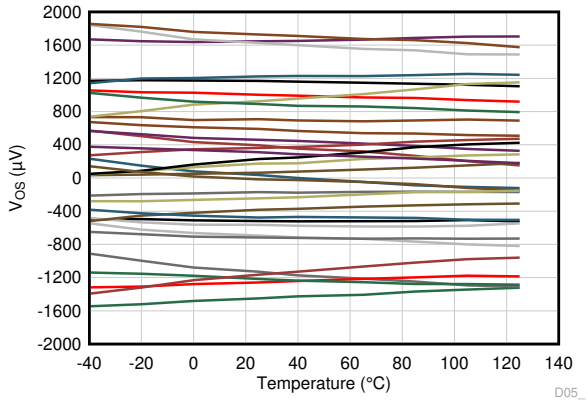

$V_S$ = 5.5V, $T_A$ = –40°C to +125°C

**Figure 5-2. Offset Voltage Drift Distribution Histogram**




$V_S$ = 5.5V, $V_{CM}$ = V–

**Figure 5-3. Input Offset Voltage vs Temperature**




$V_S$ = 5.5V, $V_{CM}$ = V+

**Figure 5-4. Input Offset Voltage vs Temperature**

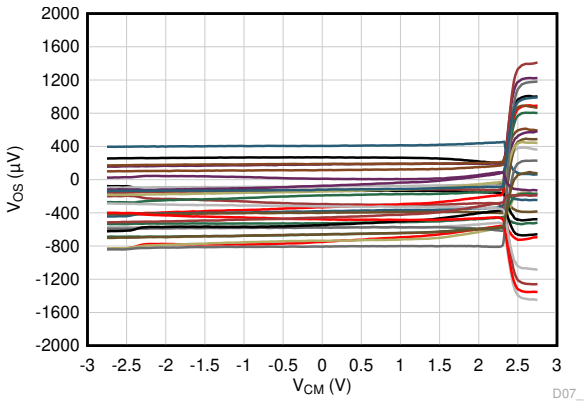
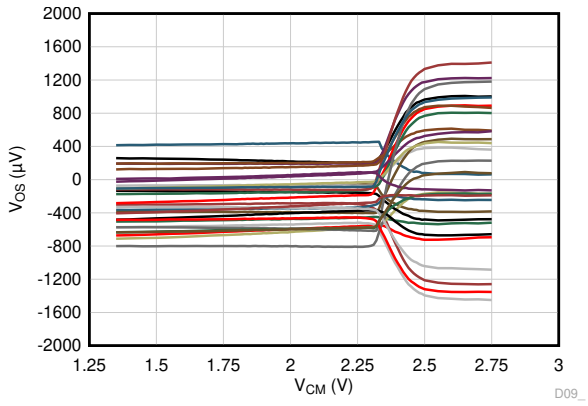



**Figure 5-5. Offset Voltage vs Common-Mode**




$V_{CM}$ > (V+) – 1.4V

**Figure 5-6. Offset Voltage vs Common-Mode**

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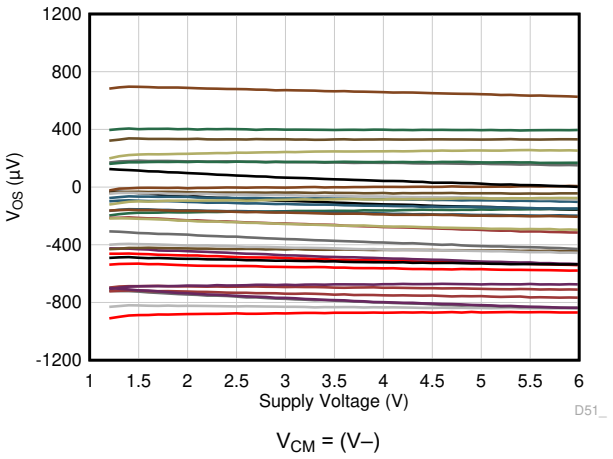
## 5.6 Typical Characteristics (continued)

at $T_A$ = 25°C, V+ = 2.75V, V– = –2.75V, $R_L$ = 10kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)




$V_{CM}$ = (V–)

**Figure 5-7. Offset Voltage vs Supply Voltage**

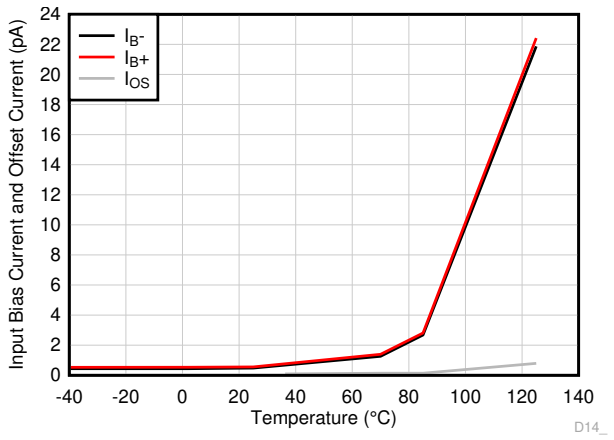



**Figure 5-8. $I_B$ and $I_{OS}$ vs Temperature**

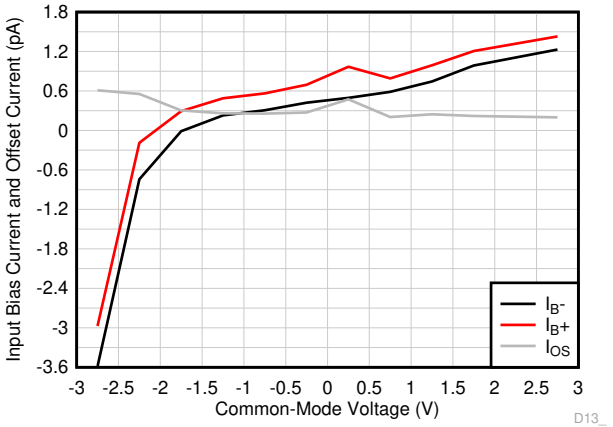



**Figure 5-9. $I_B$ and $I_{OS}$ vs Common-Mode Voltage**

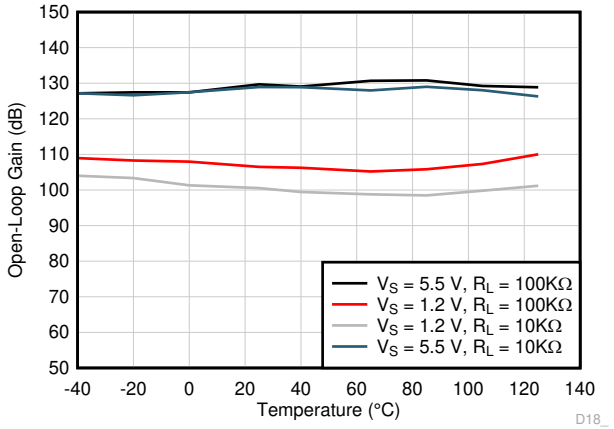
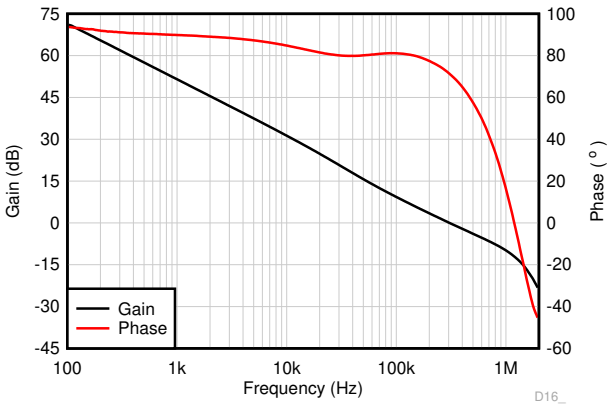



**Figure 5-10. Open-Loop Gain vs Temperature**




CL = 10pF

**Figure 5-11. Open-Loop Gain and Phase vs Frequency**

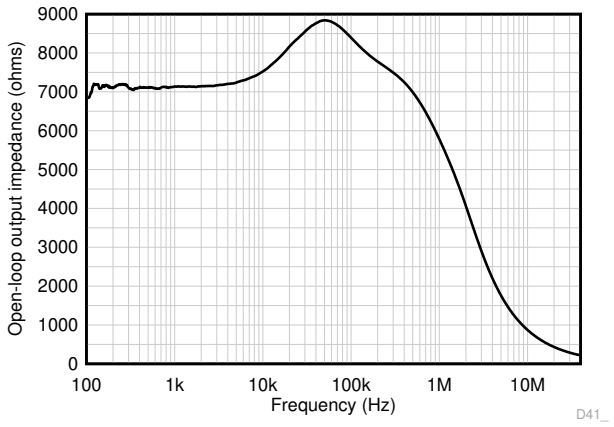
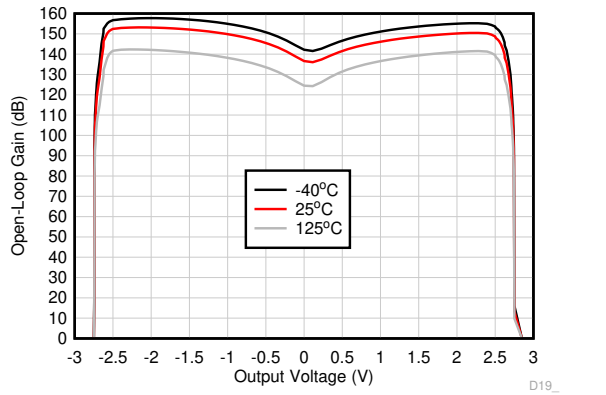



**Figure 5-12. Open-Loop Output Impedance vs Frequency**

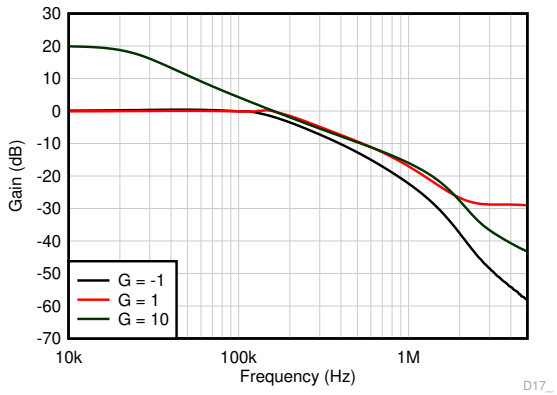
## 5.6 Typical Characteristics (continued)

at $T_A$ = 25°C, V+ = 2.75V, V– = –2.75V, $R_L$ = 10kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)



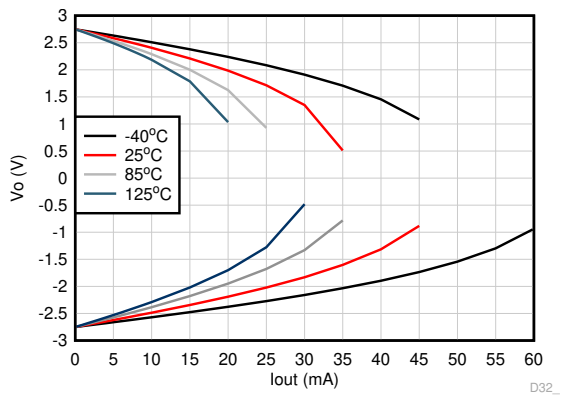

V+ = 2.75V, V– = –2.75V  $R_L$ = 10kΩ

**Figure 5-13. Open-Loop Gain vs Output Voltage**



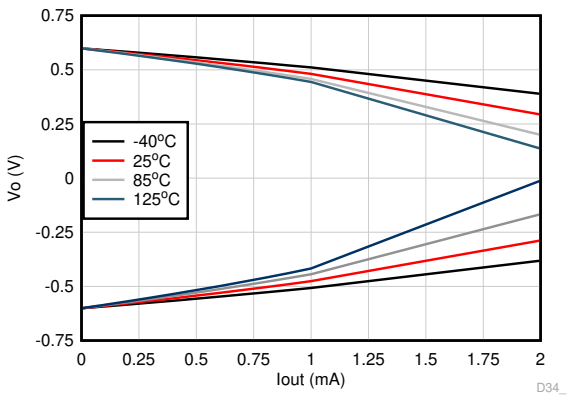

$C_L$ = 10pF

**Figure 5-14. Closed-Loop Gain vs Frequency**




V+ = 2.75V, V– = –2.75V

**Figure 5-15. Output Voltage vs Output Current (Claw)**




V+ = 0.6V, V– = –0.6V

**Figure 5-16. Output Voltage vs Output Current (Claw)**

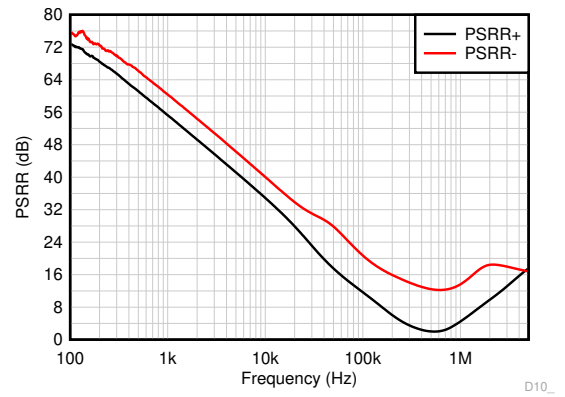
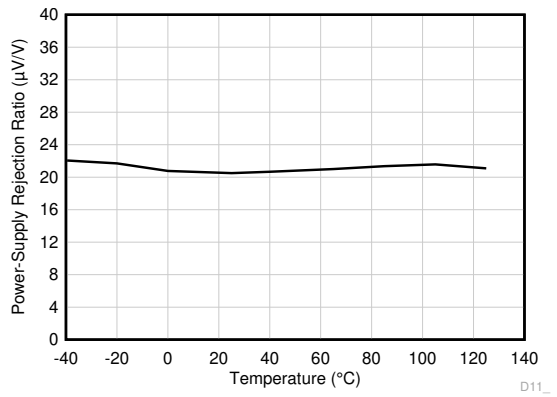



**Figure 5-17. PSRR vs Frequency**




$V_S$ = 1.2V to 5.5V

**Figure 5-18. DC PSRR vs Temperature**

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## 5.6 Typical Characteristics (continued)

at $T_A$ = 25°C, V+ = 2.75V, V– = –2.75V, $R_L$ = 10kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)

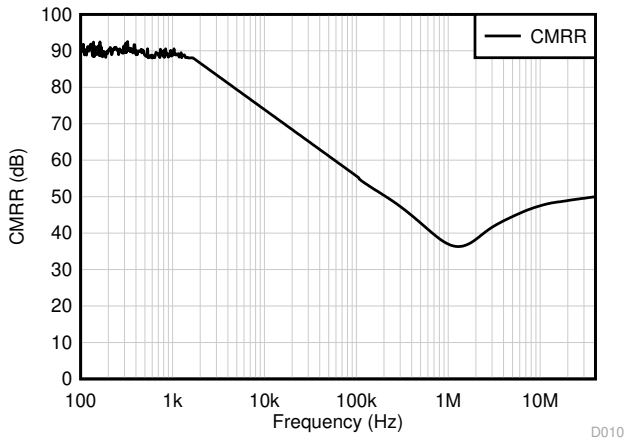



Figure 5-19. CMRR vs Frequency

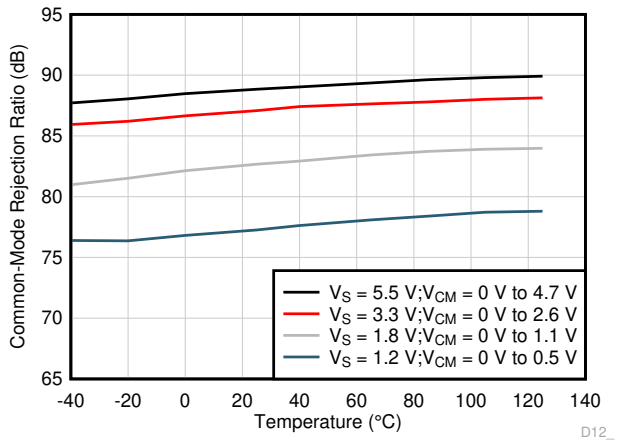



Figure 5-20. DC CMRR vs Temperature

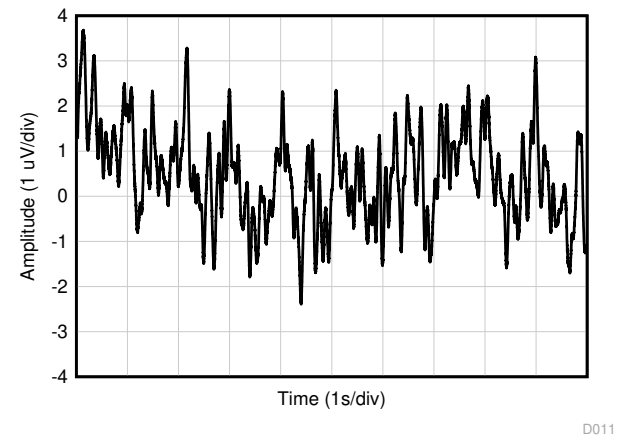



Figure 5-21. 0.1Hz to 10Hz Voltage Noise in Time Domain

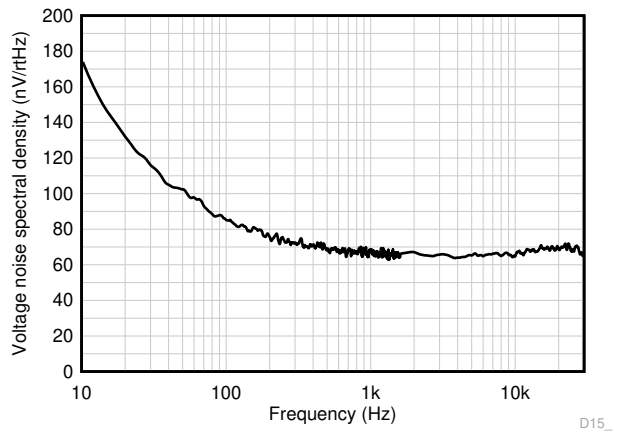
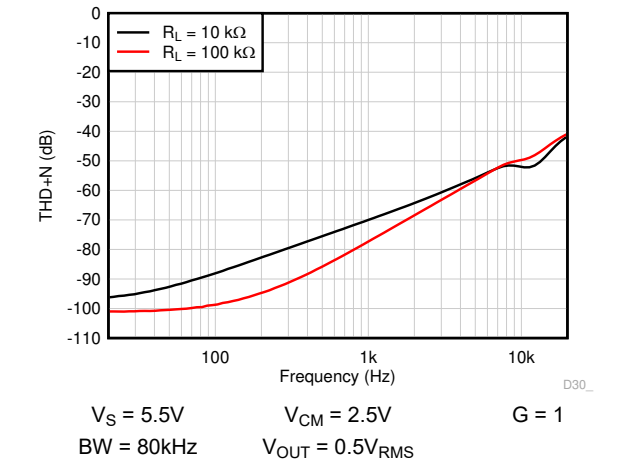
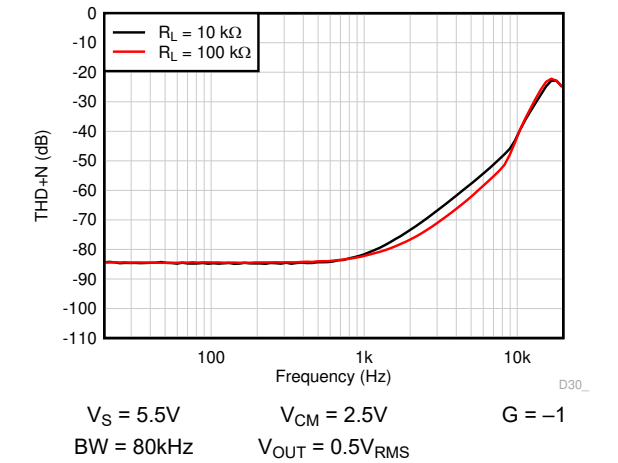



Figure 5-22. Input Voltage Noise Spectral Density




$V_S$ = 5.5V $V_{CM}$ = 2.5V G = 1
BW = 80kHz $V_{OUT}$ = 0.5$V_{RMS}$

Figure 5-23. THD + N vs Frequency

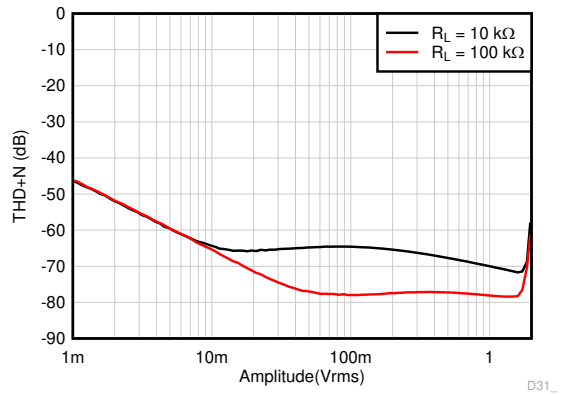



$V_S$ = 5.5V $V_{CM}$ = 2.5V G = –1
BW = 80kHz $V_{OUT}$ = 0.5$V_{RMS}$

Figure 5-24. THD + N vs Frequency

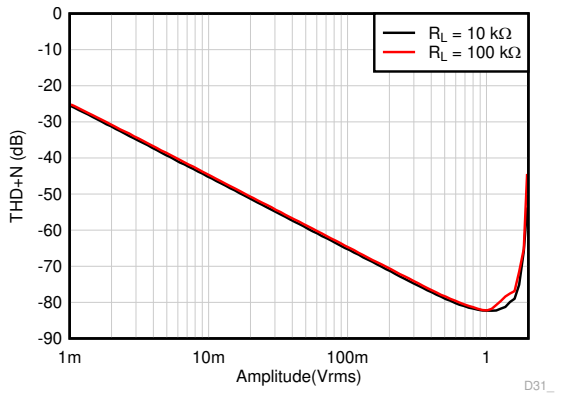
## 5.6 Typical Characteristics (continued)

at $T_A$ = 25°C, V+ = 2.75V, V– = –2.75V, $R_L$ = 10kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)




$V_S$ = 5.5V $V_{CM}$ = 2.5V f = 1kHz
G = 1 BW = 80kHz

**Figure 5-25. THD + N vs Amplitude**




$V_S$ = 5.5V $V_{CM}$ = 2.5V f = 1kHz
G = –1 BW = 80kHz

**Figure 5-26. THD + N vs Amplitude**

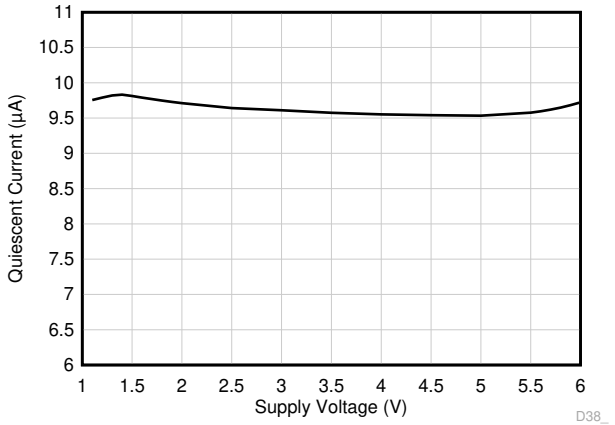



**Figure 5-27. Quiescent Current vs Supply Voltage**

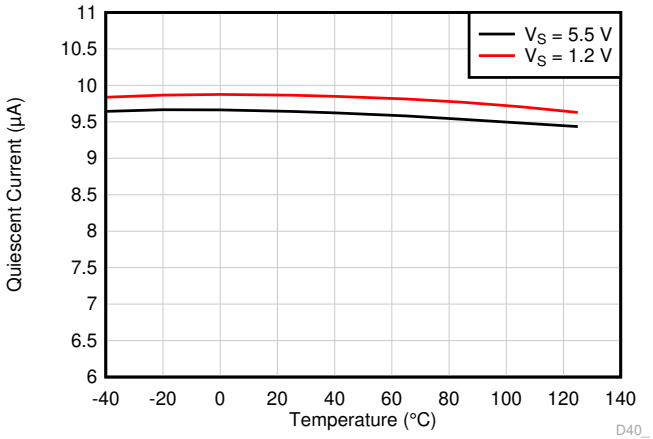
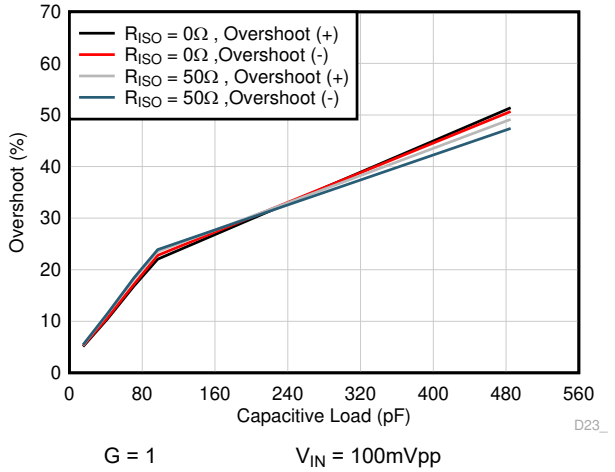
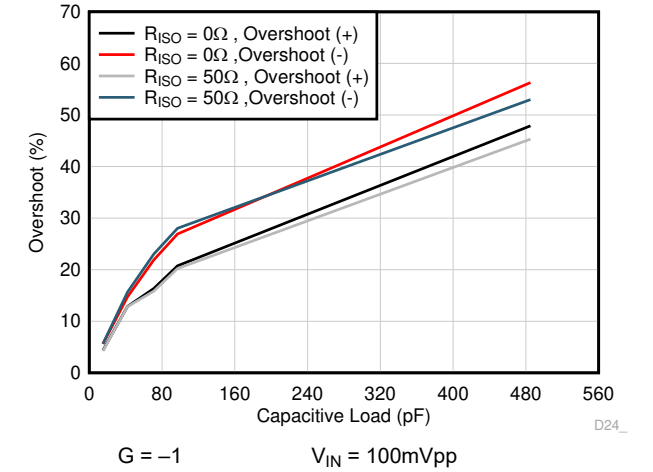



**Figure 5-28. Quiescent Current vs Temperature**




G = 1 $V_{IN}$ = 100mVpp

**Figure 5-29. Small Signal Overshoot vs Capacitive Load**




G = –1 $V_{IN}$ = 100mVpp

**Figure 5-30. Small Signal Overshoot vs Capacitive Load**

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## 5.6 Typical Characteristics (continued)

at $T_A$ = 25°C, V+ = 2.75V, V– = –2.75V, $R_L$ = 10kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)

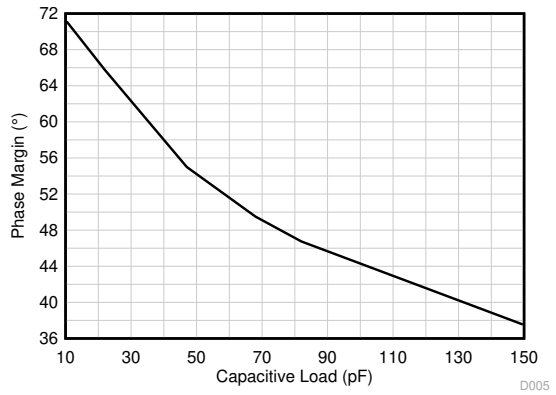
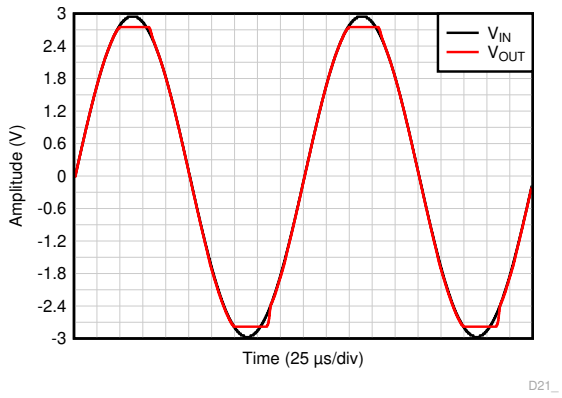
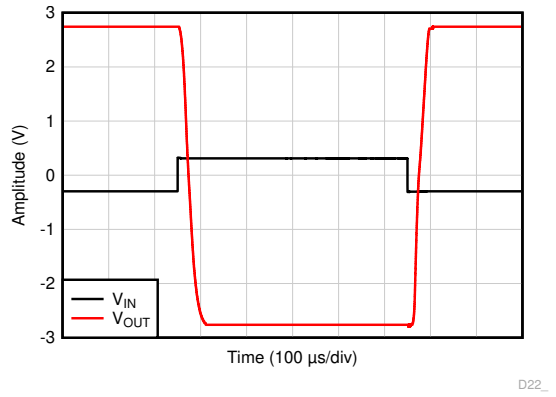



**Figure 5-31. Phase Margin vs Capacitive Load**



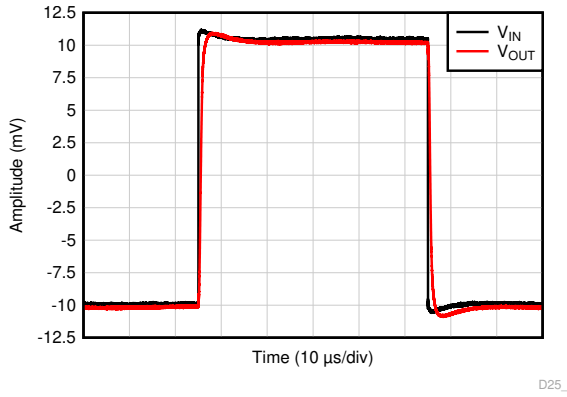

G = 1 $V_{IN}$ = 6$V_{PP}$

**Figure 5-32. No Phase Reversal**



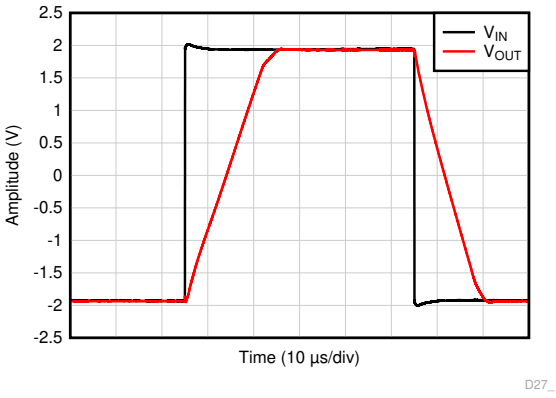

G = –10 $V_{IN}$ = 600m$V_{PP}$

**Figure 5-33. Overload Recovery**



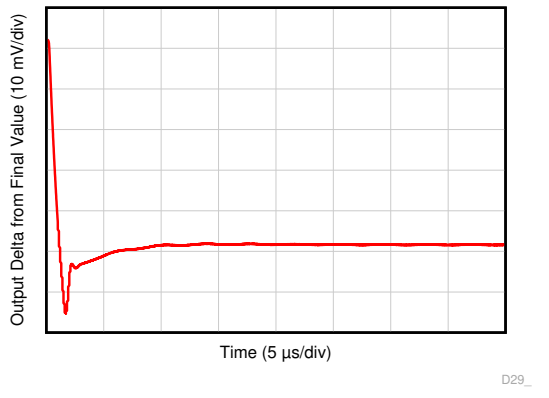

G = 1 $V_{IN}$ = 20m$V_{PP}$ $C_L$ = 10pF

**Figure 5-34. Small-Signal Step Response**




G = 1 $V_{IN}$ = 4$V_{PP}$ $C_L$ = 10pF

**Figure 5-35. Large-Signal Step Response**

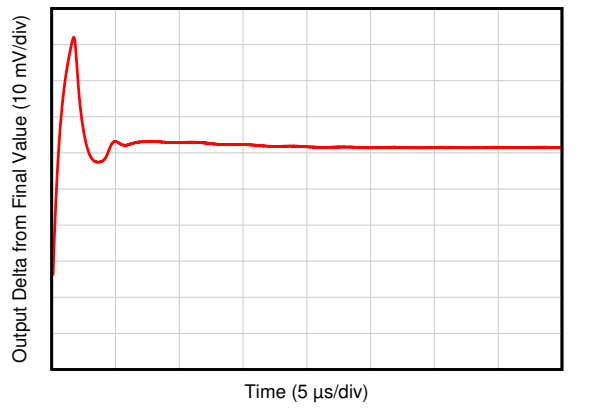



G = 1 $V_{IN}$ = 4$V_{PP}$ $C_L$ = 10pF

**Figure 5-36. Large-Signal Settling Time (Negative)**

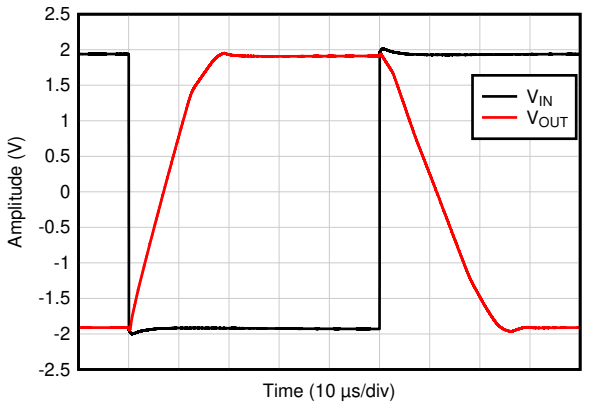
## 5.6 Typical Characteristics (continued)

at $T_A$ = 25°C, V+ = 2.75V, V– = –2.75V, $R_L$ = 10kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)




G = 1 $V_{IN}$ = 4$V_{PP}$ $C_L$ = 10pF

**Figure 5-37. Large-Signal Settling Time (Positive)**




G = –1 $V_{IN}$ = 4$V_{PP}$ $C_L$ = 10pF

**Figure 5-38. Large-Signal Step Response**

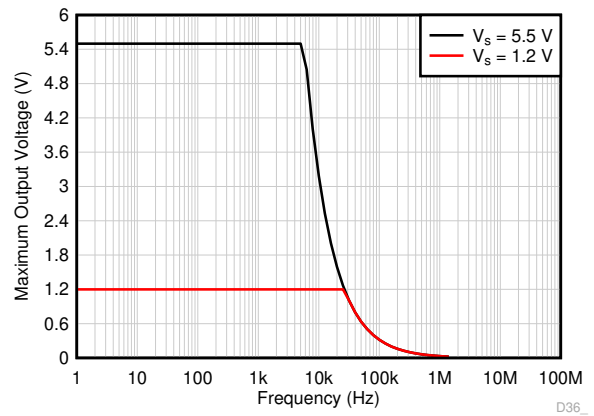



**Figure 5-39. Maximum Output Voltage vs Frequency**

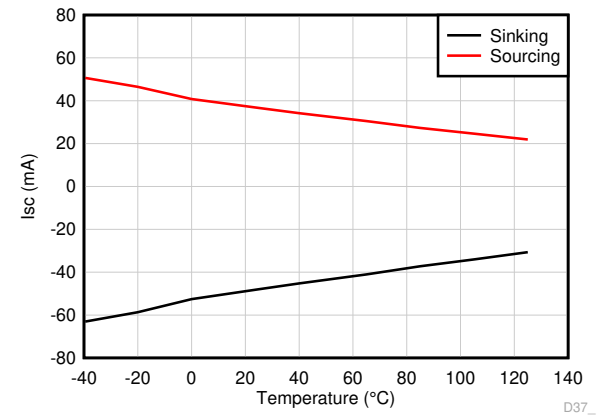



**Figure 5-40. Short-Circuit Current vs Temperature**

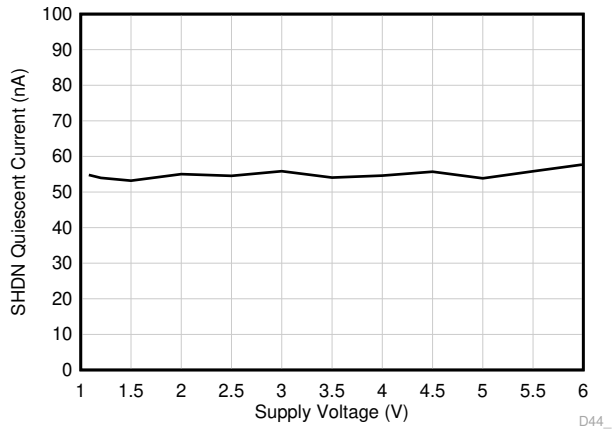



**Figure 5-41. Shutdown Mode Quiescent Current vs Supply Voltage**

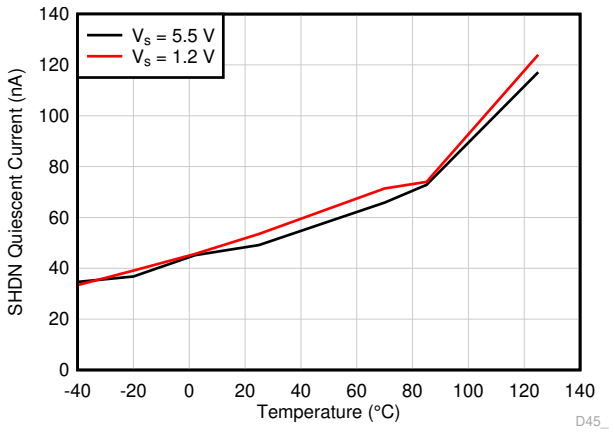



**Figure 5-42. Shutdown Mode Quiescent Current vs Temperature**

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## 5.6 Typical Characteristics (continued)

at $T_A$ = 25°C, V+ = 2.75V, V– = –2.75V, $R_L$ = 10kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)

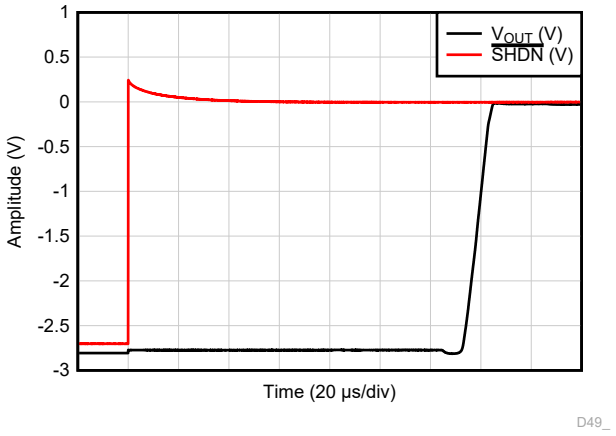


**Figure 5-43. Amplifier Enable Response**

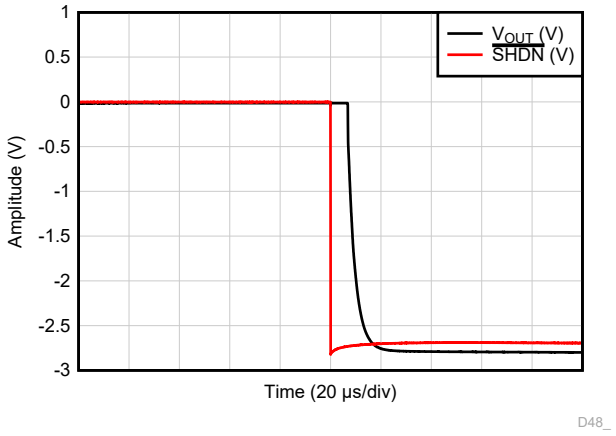


**Figure 5-44. Amplifier Disable Response**

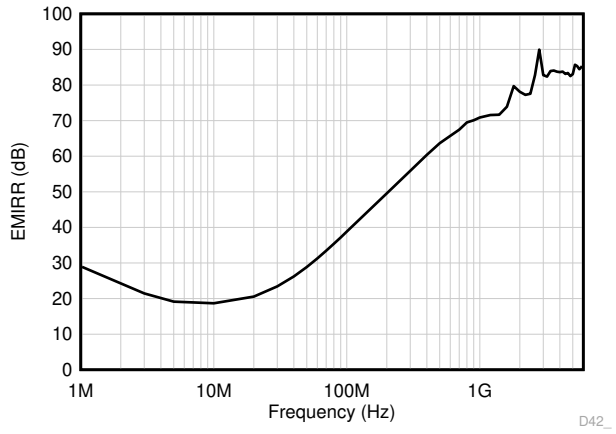


**Figure 5-45. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency**

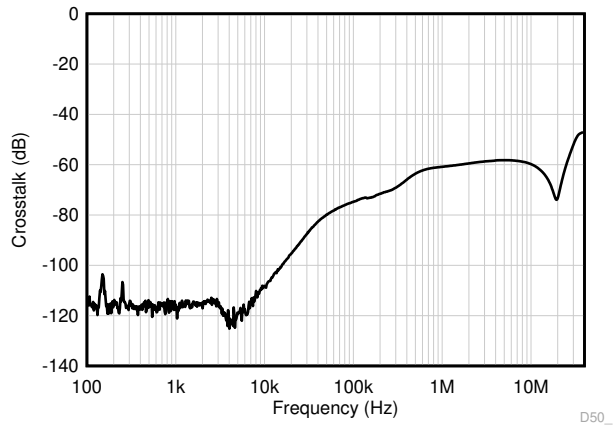


**Figure 5-46. Channel Separation**

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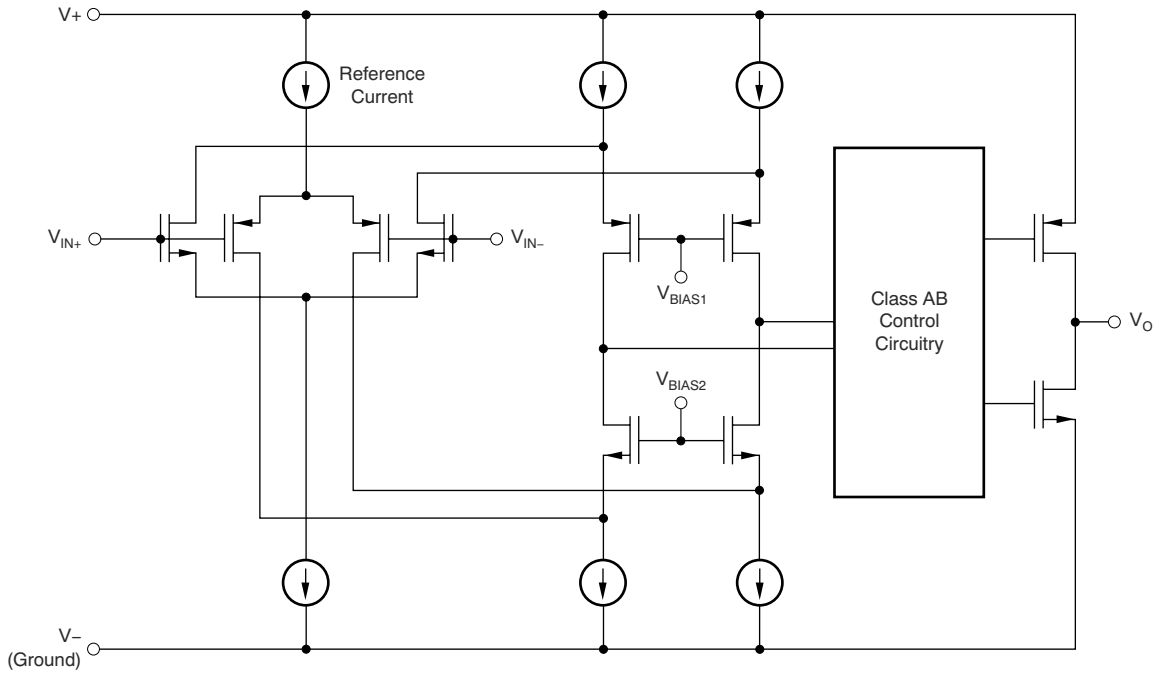
# 6 Detailed Description

## 6.1 Overview

The TLV904x-Q1 family of low-power, rail-to-rail input and output operational amplifiers are specifically designed for low-power, always-on applications. This family of amplifiers uses unique transistors that enable operation from ultra-low supply voltage of 1.2V to a standard supply voltage of 5.5V. These unity-gain stable amplifiers provide 350kHz of GBW with an $I_Q$ of only 10µA. The TLV904x-Q1 also has short-circuit current capability of 40mA at 5.5V. This combination of low voltage, low IQ, and high output current capability makes this device quite unique and an excellent choice for a wide range of general-purpose applications. The input common-mode voltage range includes both rails, and allows the TLV904x-Q1 series to be used in many single-supply or dual supply configurations. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes these devices an excellent choice for driving low-speed sampling analog-to-digital converters (ADCs). Further, the class AB output stage is capable of driving resistive loads greater than 2kΩ connected to any point between V+ and ground.

The TLV904x-Q1 can drive up to 100pF with a typical phase margin of 45° and features 350kHz gain bandwidth product, 0.2V/µs slew rate with 6.5µ$V_{p-p}$ integrated noise (0.1 to 10Hz) while consuming only 10µA supply current per channel, thus providing a good AC performance at a very low power consumption. DC applications are also well served with a low input bias current of 1pA (typical), an input offset voltage of 0.6mV (typical) and a good PSRR, CMRR, and $A_{OL}$.

## 6.2 Functional Block Diagram

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## 6.3 Feature Description

### 6.3.1 Operating Voltage

The TLV904x-Q1 series of operational amplifiers is fully specified for operation from 1.2V to 5.5V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are provided in the *Typical* Characteristics section. A ceramic capacitor with at least 0.01µF is highly recommended to bypass power-supply pins.

### 6.3.2 Rail-to-Rail Input

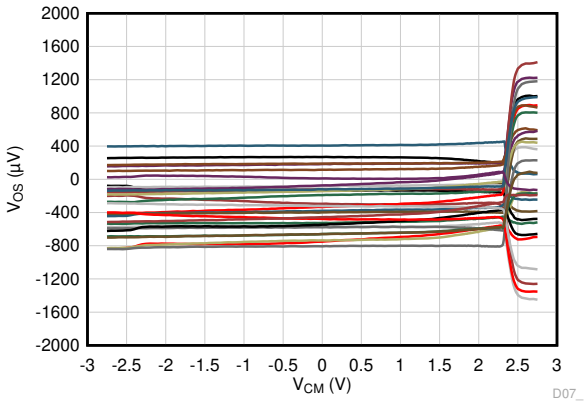
The input common-mode voltage range of the TLV904x-Q1 series extends to either supply rails. This is true even when operating at the ultra-low supply voltage of 1.2V, all the way up to the standard supply voltage of 5.5V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. Refer to *Functional Block Diagram* for more details.

For most amplifiers with a complementary input stage, one of the input pairs, usually the P-channel input pair, is designed to deliver slightly better performance in terms of input offset voltage, offset drift over the N-channel pair. Consequently, the P-channel pair is designed to cover the majority of the common-mode range with the N-channel pair slated to slowly take over at a certain threshold voltage from the positive rail. Just after the threshold voltage, both the input pairs are in operation for a small range referred to as the transition region. Beyond this region, the N-channel pair completely takes over. Within the transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region. Hence, most applications generally prefer operating in the P-channel input range where the performance is slightly better.

For the TLV904x-Q1, the P-channel pair is typically active for input voltages from the negative rail to (V+) – 0.4V and the N-channel pair is typically active for input voltages from the positive supply to (V+) – 0.4V. The transition region occurs typically from (V+) – 0.5V to (V+) – 0.3V, in which both pairs are on. These voltage levels mentioned above can vary with process variations associated with threshold voltage of transistors. In the TLV904x-Q1, 200mV transition region mentioned above can vary up to 200mV in either direction. Thus, the transition region (both stages on) can range from (V+) – 0.7V to (V+) – 0.5V on the low end, up to (V+) – 0.3V to (V+) – 0.1V on the high end.

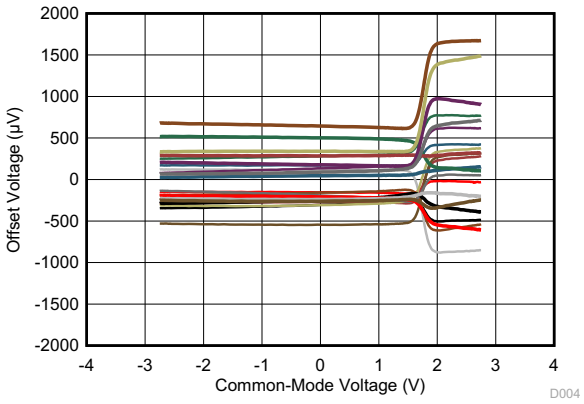
Recollecting the fact that a P-channel input pair usually offers better performance over a N-channel input pair, the TLV904x-Q1 is designed to offer a much wider P-channel input pair range, in comparison to most complimentary input amplifiers in the industry. A side-by-side comparison of the TLV904x-Q1 and the TLV900x-Q1 is provided below. Note that the TLV900x-Q1 is designed to have P-channel pair operation only until 1.4V from the positive rail while the TLV904x-Q1 is designed to have P-channel pair operation all the way till 0.7V from the positive rail. This additional 700mV of P-channel input pair range for the TLV904x-Q1 is particularly useful when operating at lower supply voltages (1.2V, 1.8V, and so forth) where the P-channel input range usually gets limited to a great extent.

Thus the wide common-mode swing of input signal can be accommodated more easily within the P-channel input pair of the TLV904x-Q1, while likely avoiding the transition region, thereby maintaining linearity.




V+ = 2.75V, V– = –2.75V

**Figure 6-1. TLV904x-Q1 Offset Voltage vs Common-Mode Voltage**




V+ = 2.75V, V– = –2.75V

**Figure 6-2. TLV900x-Q1 Offset Voltage vs Common-Mode Voltage**

### *6.3.3 Rail-to-Rail Output*

Designed as a micro-power, low-noise operational amplifier, the TLV904x-Q1 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 5kΩ, the output typically swings to within 20mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails.

### *6.3.4 Common-Mode Rejection Ratio (CMRR)*

The CMRR for the TLV904x-Q1 is specified in several ways so the best match for a given application can be used; see the *Electrical Characteristics* table. First, the CMRR of the device in the common-mode range below the transition region [VCM < (V+) – 0.7V] is given. This specification is the best indicator of the capability of the device when the application requires using one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at (VCM = 0V to 5.5V). This last value includes the variations measured through the transition region.

### *6.3.5 Capacitive Load and Stability*

The TLV904x-Q1 is designed for applications where driving a capacitive load is required. As with all operational amplifiers, there are specific instances where the TLV904x-Q1 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in the unity-gain configuration, the TLV904x-Q1 remains stable with a pure capacitive load up to approximately 100pF with a good phase margin of 45° typical. The equivalent series resistance (ESR) of some very large capacitors ($C_L$ greater than 1µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically 10Ω to 20Ω) in series with the output, as shown in Figure 6-3. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

ADVANCE INFORMATION

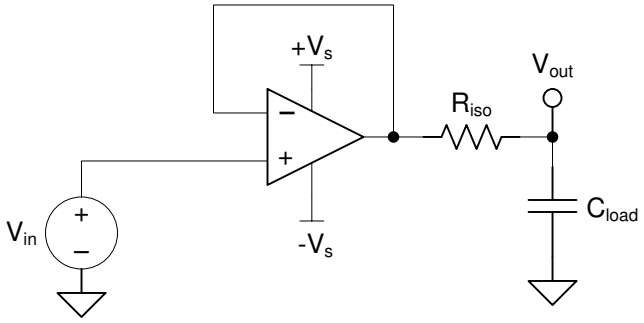



**Figure 6-3. Improving Capacitive Load Drive**

### *6.3.6 Overload Recovery*

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. After one of the output devices enters the saturation region, the output stage requires additional time to return to the linear operating state which is referred to as overload recovery time. After the output stage returns to the linear operating state, the amplifier begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV904x-Q1 family is approximately 13µs typical.

### *6.3.7 EMI Rejection*

The TLV904x-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV904x-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 6-4 shows the results of this testing on the TLV904x-Q1. Table 6-1 shows the EMIRR IN+ values for the TLV904x-Q1 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application note contains detailed information on how EMIRR performance relates to op amps and is available for download from www.ti.com.

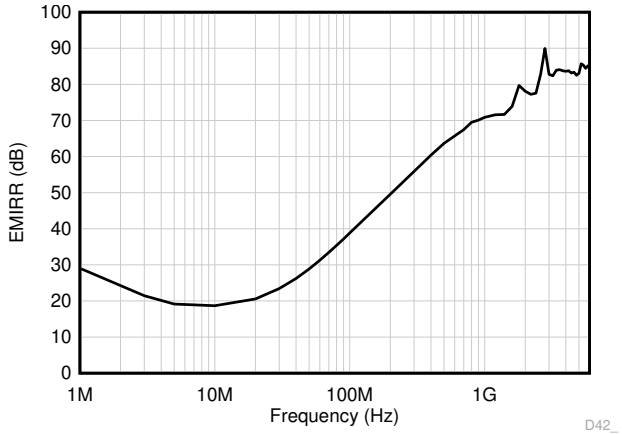



**Figure 6-4. EMIRR Testing**

**Table 6-1. TLV904x-Q1 EMIRR IN+ for Frequencies of Interest**

| FREQUENCY | APPLICATION OR ALLOCATION | EMIRR IN+ |
|---|---|---|
| 400MHz | Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications | 60dB |
| 900MHz | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications | 70dB |
| 1.8GHz | GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2GHz) | 75dB |
| 2.4GHz | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz) | 79dB |
| 3.6GHz | Radiolocation, aero communication and navigation, satellite, mobile, S-band | 82dB |
| 5GHz | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz) | 85dB |

### *6.3.8 Electrical Overstress*

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 6-5 shows the ESD circuits contained in the TLV904x-Q1 devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where the connections meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

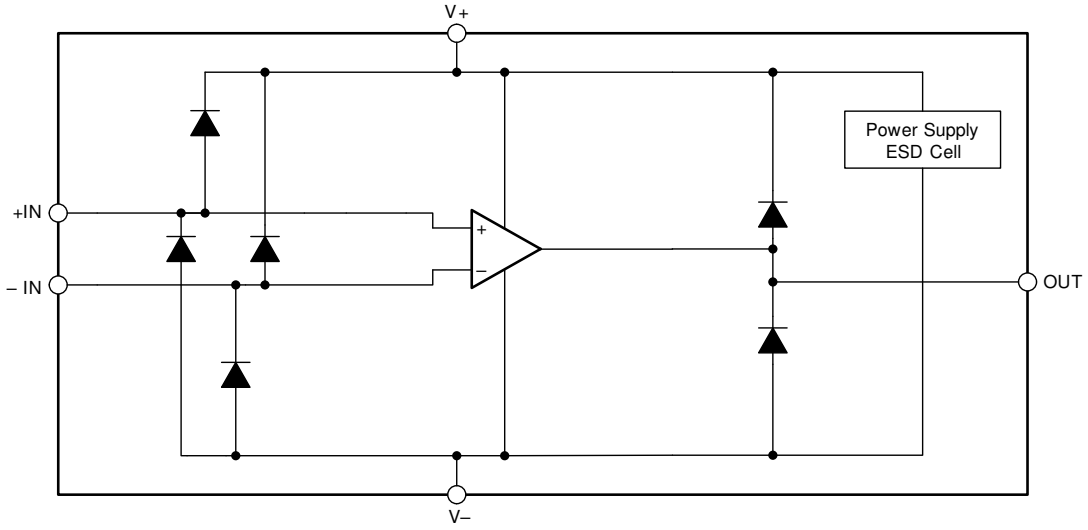



**Figure 6-5. Equivalent Internal ESD Circuitry**

### *6.3.9 Input and ESD Protection*

The TLV904x-Q1 family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10mA. Figure 6-6 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

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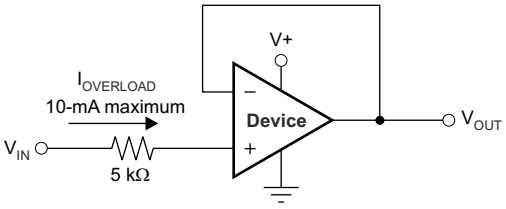


**Figure 6-6. Input Current Protection**

## 6.4 Device Functional Modes

The TLV904x-Q1 devices have a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.2V (±0.6V) and 5.5V (±2.75V).

ADVANCE INFORMATION

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

The TLV904x-Q1 family of low-power, rail-to-rail input and output operational amplifiers is specifically designed for lower power applications. The devices operate from 1.2V to 5.5V, are unity-gain stable, and are an excellent choice for a wide range of general-purpose applications. The class AB output stage is capable of driving resistive loads greater than 2kΩ connected to any point between V+ and V–. The input common-mode voltage range includes both rails and allows the TLV904x-Q1 series to be used in many single-supply or dual supply configurations.

## 7.2 Typical Application

### *7.2.1 TLV904x-Q1 Low-Side, Current Sensing Application*

Figure 7-1 shows the TLV904x-Q1 configured in a low-side current sensing application.

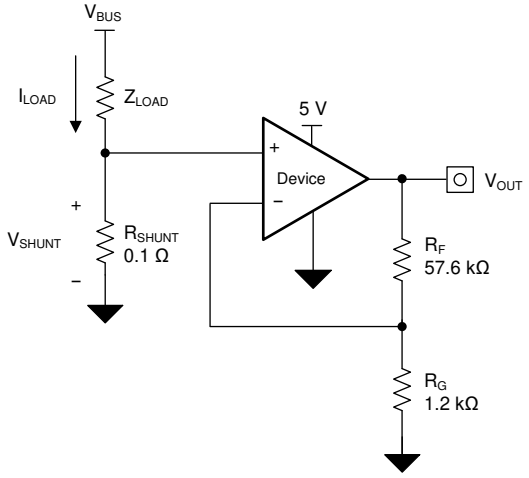


**Figure 7-1. TLV904x-Q1 in a Low-Side, Current-Sensing Application**

ADVANCE INFORMATION

#### 7.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Maximum output voltage: 4.9V
- Maximum shunt voltage: 100mV

#### 7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 7-1 is given in Equation 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current ($I_{LOAD}$) produces a voltage drop across the shunt resistor ($R_{SHUNT}$). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is shown using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \tag{2}$$

Using Equation 2, $R_{SHUNT}$ is calculated to be 100mΩ. The voltage drop produced by $I_{LOAD}$ and $R_{SHUNT}$ is amplified by the TLV904x-Q1 to produce an output voltage of approximately 0V to 4.9V. Use Equation 3 to calculate the gain the TLV904x-Q1 requires to product the necessary output voltage.

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \tag{3}$$

Using Equation 3, the required gain in this example is 49V/V, which is set with resistors $R_F$ and $R_G$. Equation 4 sizes the resistors $R_F$ and $R_G$ to set the gain of the TLV904x-Q1 to 49V/V.

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \tag{4}$$

Selecting $R_F$ as 57.6kΩ and $R_G$ as 1.2kΩ provides a combination that equals 49V/V. Figure 7-2 shows the measured transfer function of the circuit shown in Figure 7-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no single impedance selection that works for every system; you must choose an impedance that is designed for your system parameters.

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#### 7.2.1.3 Application Curve

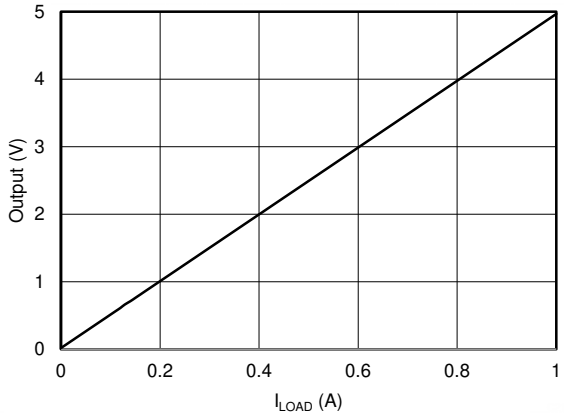


**Figure 7-2. Low-Side, Current-Sense Transfer Function**

## 7.3 Power Supply Recommendations

The TLV904x-Q1 family is specified for operation from 1.2V to 5.5V (±0.6V to ±2.75V); many specifications apply from –40°C to 125°C. *Electrical Characteristics* presents parameters that exhibit significant variance with regard to operating voltage or temperature.

**CAUTION**

Supply voltages larger than 6V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place a 0.1µF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines*.

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## 7.4 Layout

### *7.4.1 Layout Guidelines*

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Remember that noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separating grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in *Layout Example*. Keep $R_F$ and $R_G$ close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

### 7.4.2 Layout Example

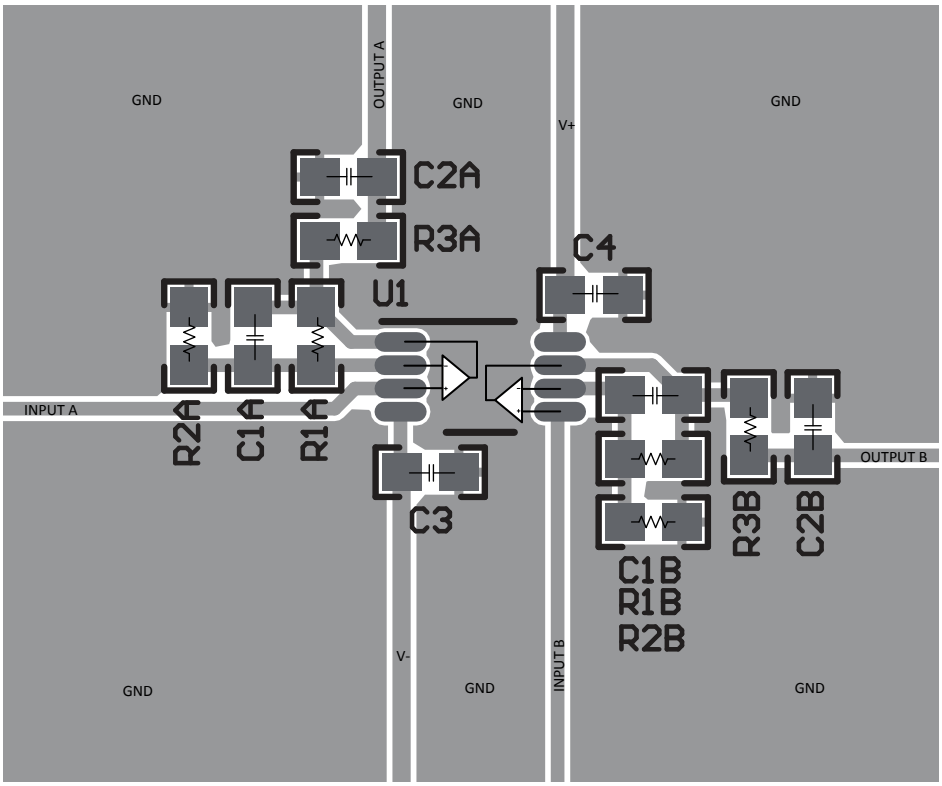


**Figure 7-3. Example Layout for VSSOP-8 (DGK) Package**

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# 8 Device and Documentation Support

## 8.1 Documentation Support

### *8.1.1 Related Documentation*

For related documentation see the following:

- Texas Instruments, *Designing with Low-power Op Amps, Part 1: Power-saving Techniques for Op-amp Circuits* technical article
- Texas Instruments, *Designing with Low-power Op Amps, Part 2: Low-power Op Amps for Low-supply-voltage Applications* technical article
- Texas Instruments, *Designing with Low-power Op Amps, Part 3: Saving Power with the Shutdown Amplifier* technical article
- Texas Instruments, *Designing with Low-power Op Amps, Part 4: Stability Concerns and Solutions* technical article
- Texas Instruments, *EMI rejection ratio of operational amplifiers* application note

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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## 8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

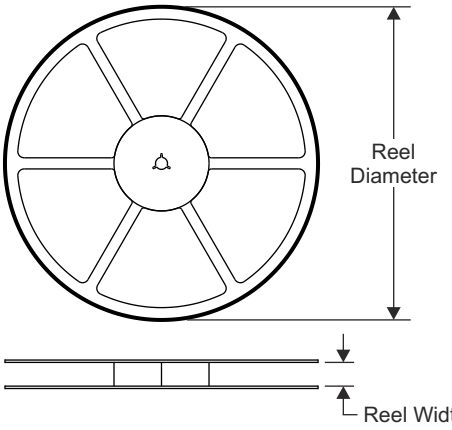
| DATE | REVISION | NOTES |
|---|---|---|
| June 2024 | * | Initial Release |

# 10 Mechanical, Packaging, and Orderable Information

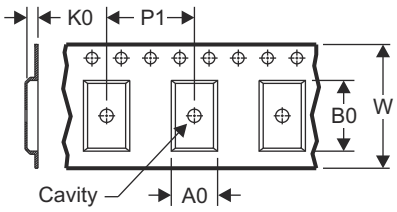
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 10.1 Tape and Reel Information

**REEL DIMENSIONS**

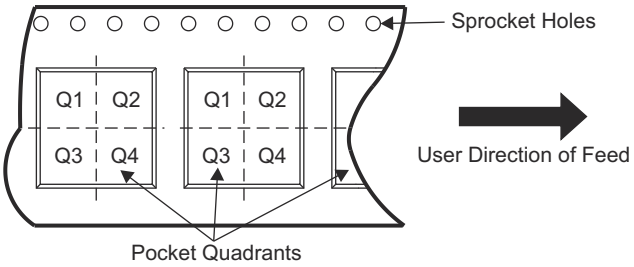



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PTLV9044QPWRQ1 | TSSOP | PW | 14 | 3000 | 330 | 12.4 | 6.9 | 5.6 | 1.6 | 8 | 12 | |

ADVANCE INFORMATION

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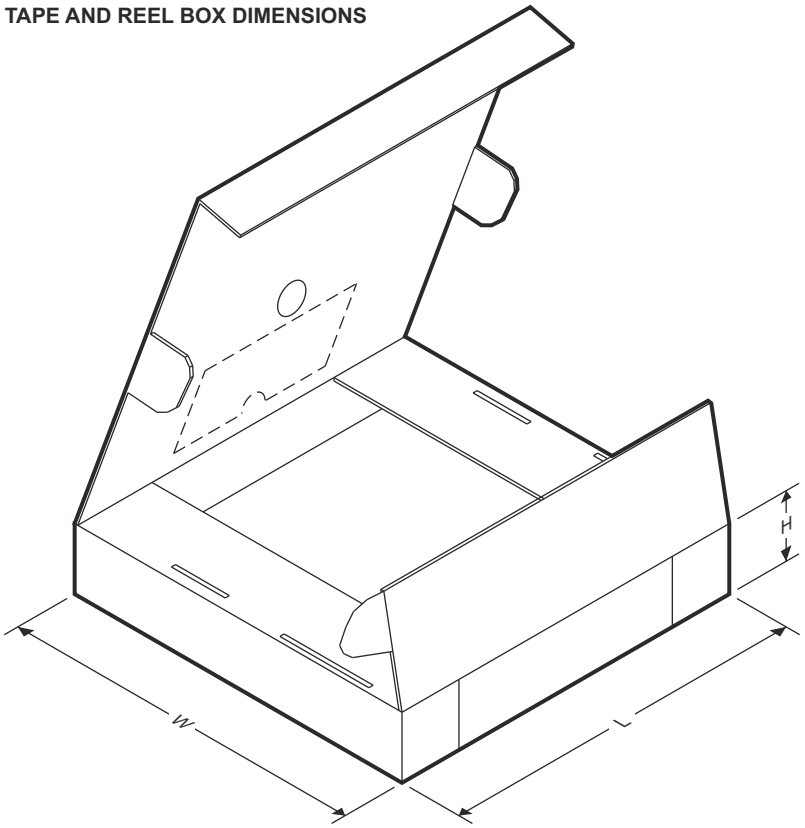
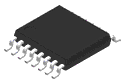
**TAPE AND REEL BOX DIMENSIONS**




| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| PTLV9044QPWRQ1 | TSSOP | PW | 14 | 3000 | 356 | 356 | 35 |

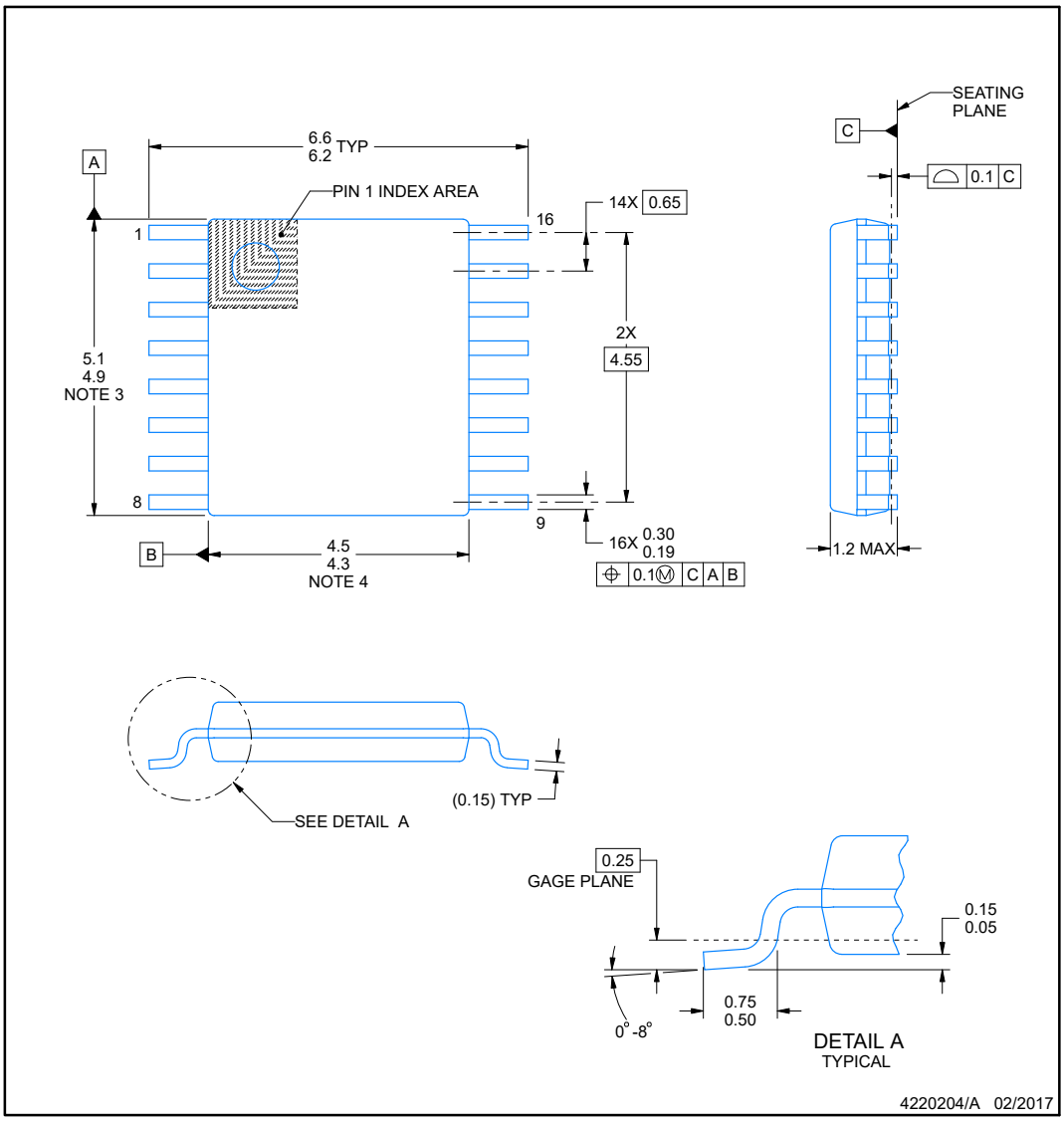
# PACKAGE OUTLINE

## PW0016A



## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

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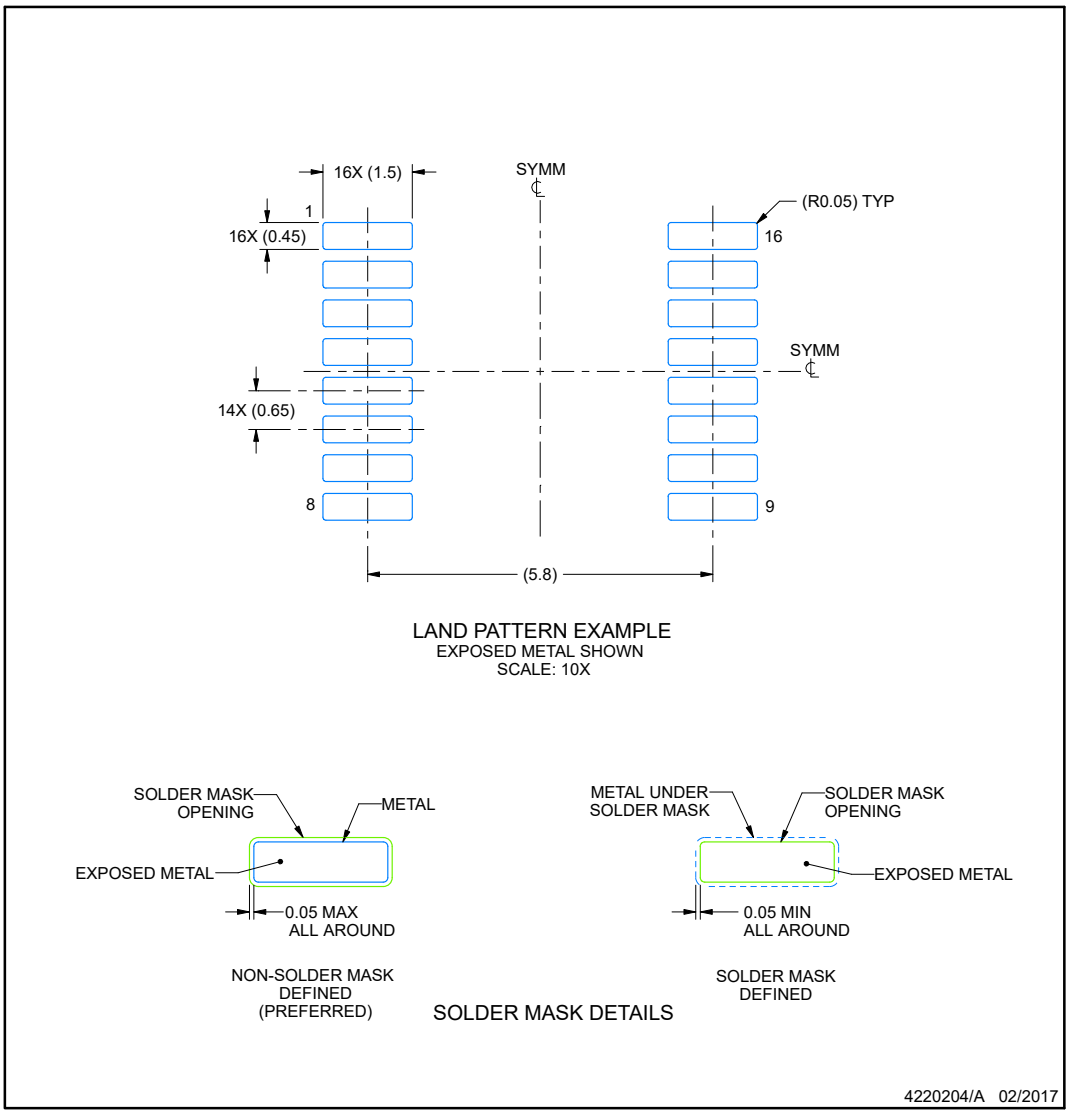
## EXAMPLE BOARD LAYOUT

**PW0016A** — **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



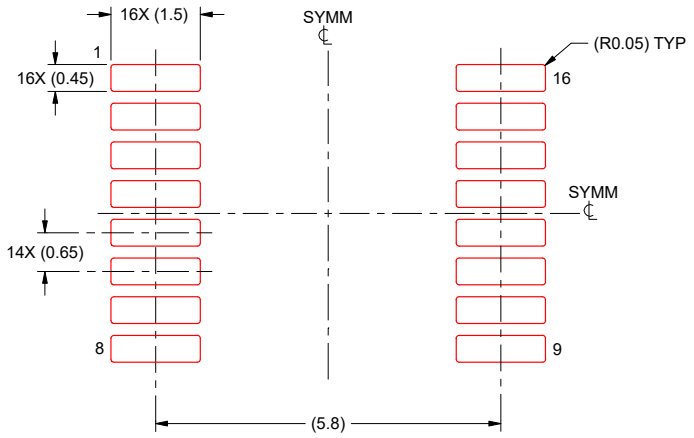

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**PW0016A** — **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PTLV9044QPWRQ1 | ACTIVE | TSSOP | PW | 14 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



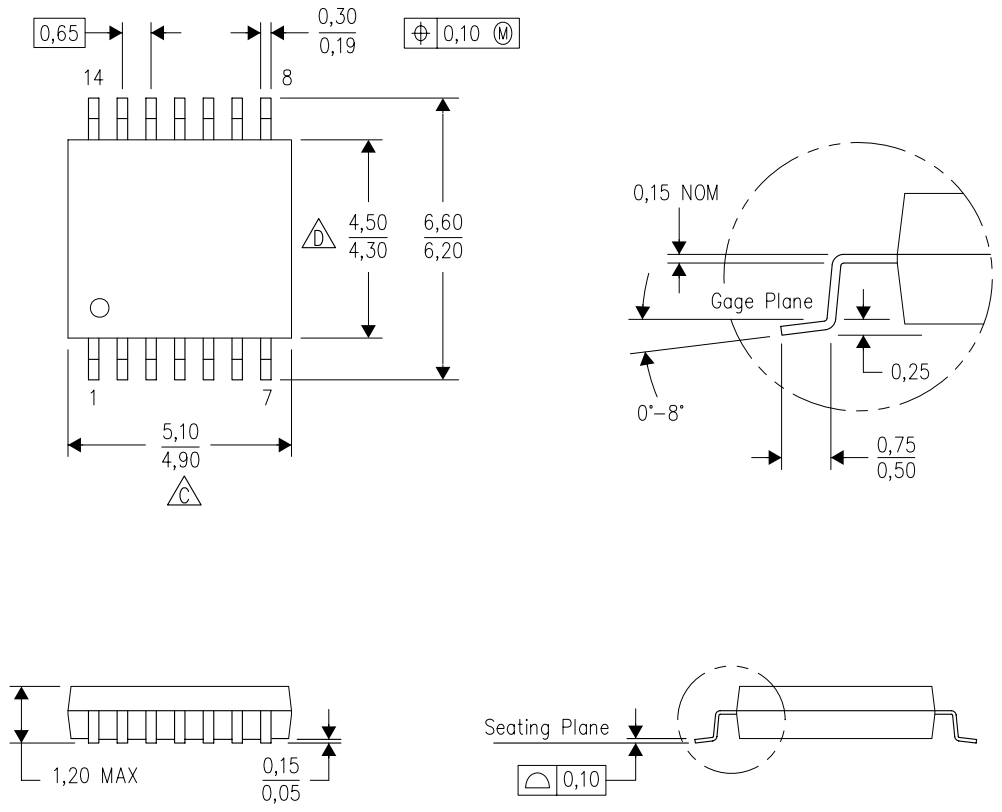
**OTHER QUALIFIED VERSIONS OF TLV9044-Q1 :**

- Catalog : TLV9044

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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