OPA4991-EP 采用增强型塑料封装的 40V 轨到轨输入/输出、低失调电压、低噪声运算放大器

1 特性

- 增强型塑料
  - 单受控基线
  - 制造、组装和测试一体化基地
  - 金线
  - NiPdAu 铅涂层
  - 支持军用（–55°C 至 125°C）温度范围
  - 延长了产品生命周期
  - 延长了产品变更通知
  - 产品可追溯性
  - 采用增强型模塑化合物实现低释气
- 低失调电压：±125μV
- 低噪声：1 kHz 时为 10.8nV/√Hz
- 高共模抑制：130dB
- 低偏置电流：±10pA
- 轨至轨输入和输出
- 宽带宽：4.5MHz GBW
- 高压摆率：21V/μs
- 高容性负载驱动：1nF
- 支持多路复用器/比较器的输入
- 低静态电流：每个放大器 560μA
- 宽电源电压：±1.35V 至 ±20V，2.7V 至 40V
- 强大的 EMIRR 性能：输入引脚和电源引脚上采用 EMI/RFI 滤波器

2 应用

- 陆地移动无线电
- 声纳
- 低功率音频前置放大器
- 多路复用数据采集系统
- 测试和测量设备
- ADC 驱动器放大器
- SAR ADC 基准缓冲器
- 可编程逻辑控制器
- 高侧和低侧电流感测

3 说明

OPA4991-EP 是一款采用增强型塑料封装的高电压 (40V) 通用运算放大器。该器件具有出色的直流精度和交流性能，包括轨至轨输入/输出、低失调电压（典型值为 ±125μV）、低温漂（典型值为 ±0.3μV/°C）、低噪声（10.8nV/√Hz 和 1.8μV_{PP}）和 4.5MHz 带宽。

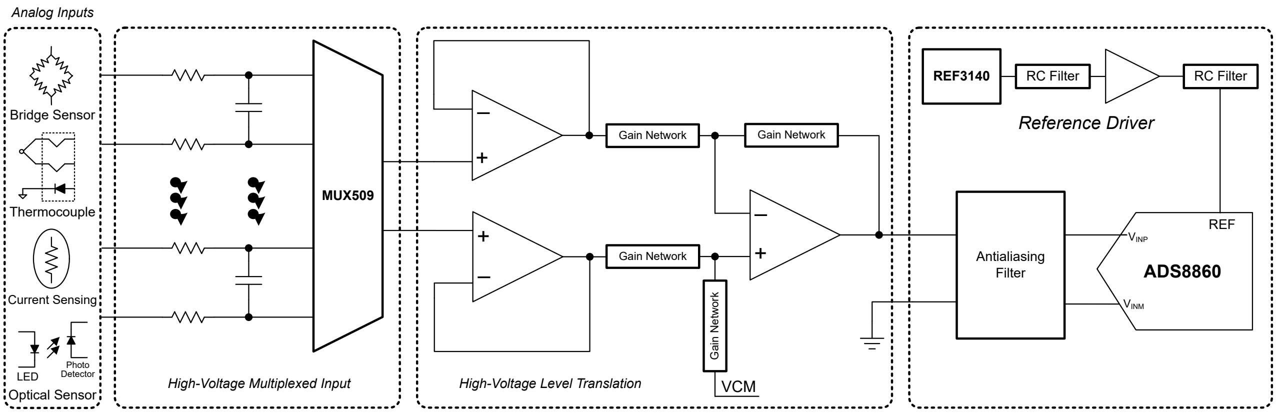
OPA4991-EP 具有独特功能，例如电源轨的差分和共模输入电压范围、高输出电流 (±75mA)、高压摆率 (21V/μs) 和高容性负载驱动 (1nF)，是一款稳定可靠的高性能运算放大器，适用于高电压应用。

OPA4991-EP 采用 SOT-23 (DYY) 封装，额定温度范围为 -55°C 至 125°C。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
OPA4991-EP	SOT-23 (14)	4.20mm × 1.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



高压信号链中的 **OPA4991-EP**

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

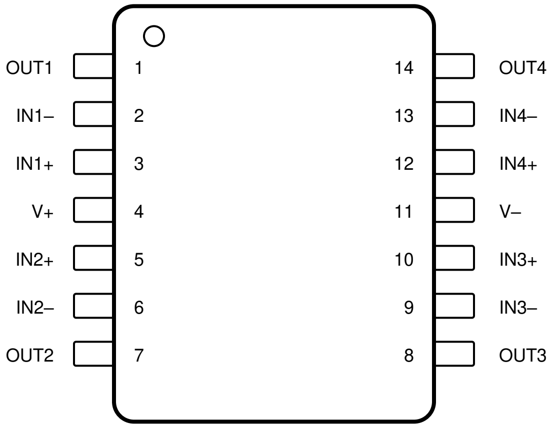
Changes from Revision A (August 2022) to Revision B (November 2022) **Page**

- 更新了热阻值.......... 4
- Increased maximum output voltage swing (Vs = 40 V, RL = 10 k) from 55 mV to 70 mV.......... 5

Changes from Revision * (June 2022) to Revision A (August 2022) **Page**

- 将器件状态从*预告信息* 更改为*量产数据* 1
- 删除了*器件信息* 表中 SOT-23 (14) 封装的预览说明.......... 1

5 Pin Configuration and Functions



Not to scale

图 5-1. OPA4991-EP DYY Package 14-Pin SOT-23 (Top View)

表 5-1. Pin Functions: OPA4991-EP

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1 –	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2 –	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3 –	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4 –	13	I	Inverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V –	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	42	V
Signal input pins	Common-mode voltage (3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage (3)		V_S + 0.2	V
	Current (3)	–10	10	mA
Output short-circuit (2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings,* the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package. This device has been designed to limit *electrical* damage due to excessive output current, but extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual *thermal* destruction. See the *节 7.3.3* for more information.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	2.7	40	V
V_I	Input voltage range	(V–) – 0.1	(V+) + 0.1	V
T_A	Specified ambient temperature	–55	125	°C

6.4 四通道器件的热性能信息

热指标 (1)		OPA4991-EP	单位
		DYY (SOT-23)	
		14 引脚	
$R_{\theta JA}$	结至环境热阻	121.6	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	53.6	°C/W
$R_{\theta JB}$	结至电路板热阻	47.8	°C/W
ψ_{JT}	结至顶部特征参数	2.1	°C/W
ψ_{JB}	结至电路板特征参数	47.6	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告，SPRA953。

6.5 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±125	±895	μV
			T_A = – -55°C to 125°C			±925	
dV_{OS}/dT	Input offset voltage drift		T_A = – -55°C to 125°C		±0.3		μV/℃
PSRR	Input offset voltage versus power supply	V_{CM} = V–, V_S = 4 V to 40 V	T_A = – -55°C to 125°C		±0.3	±1	μV/V
		V_{CM} = V–, V_S = 2.7 V to 40 V[2]			±1	±5	
	Channel separation	f = 0 Hz			5		μV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±10		pA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			1.8		$μV_{PP}$
					0.3		$μV_{RMS}$
e_N	Input voltage noise density	f = 1 kHz			10.8		nV/ $\sqrt{Hz}$
		f = 10 kHz			9.4		
i_N	Input current noise	f = 1 kHz			82		fA/ $\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 40 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V (Main input pair)	T_A = – -55°C to 125°C	107	130		dB
		V_S = 4 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V (Main input pair)		82	100		
		V_S = 2.7 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V (Main input pair)[2]		75	95		
		V_S = 2.7 V to 40 V, (V+) – 1 V < V_{CM} < (V+) + 0.1 V (Aux input pair)			85		
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 9		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40 V, V_{CM} = V– (V–) + 0.1 V < V_O < (V+) – 0.1 V		120	145		dB
			T_A = – -55°C to 125°C		142		
		V_S = 4 V, V_{CM} = V– (V–) + 0.1 V < V_O < (V+) – 0.1 V		104	130		
			T_A = – -55°C to 125°C		125		
		V_S = 2.7 V, V_{CM} = V– (V–) + 0.1 V < V_O < (V+) – 0.1 V[2]		101	120		
			T_A = – -55°C to 125°C		118		

6.5 Electrical Characteristics (continued)

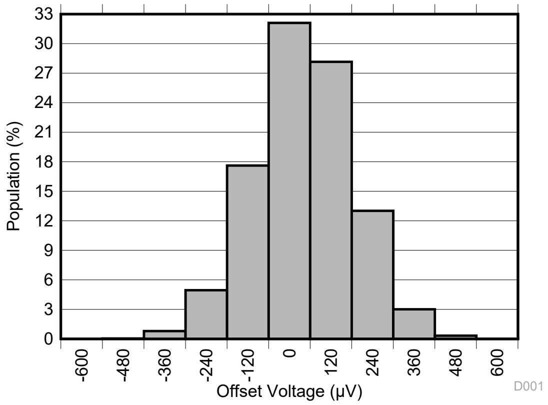
For V_S = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				4.5		MHz
SR	Slew rate	V_S = 40 V, G = +1, C_L = 20 pF			21		V/µs
t_S	Settling time	To 0.01%, V_S = 40 V, V_{STEP} = 10 V , G = +1, C_L = 20 pF			2.5		µs
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V , G = +1, C_L = 20 pF			1.5		
		To 0.1%, V_S = 40 V, V_{STEP} = 10 V , G = +1, C_L = 20 pF			2		
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V , G = +1, C_L = 20 pF			1		
	Phase margin	G = +1, R_L = 10 kΩ, C_L = 20 pF			60		°
	Overload recovery time	V_{IN} × gain > V_S			400		ns
THD+N	Total harmonic distortion + noise (1)	V_S = 40 V, V_O = 3 V_{RMS}, G = 1, f = 1 kHz			0.00021%		
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 40 V, R_L = no load(2)		5	10	mV
			V_S = 40 V, R_L = 10 kΩ		50	70	
			V_S = 40 V, R_L = 2 kΩ		300	350	
			V_S = 2.7 V, R_L = no load(2)		1	6	
			V_S = 2.7 V, R_L = 10 kΩ		5	12	
			V_S = 2.7 V, R_L = 2 kΩ		25	40	
I_{SC}	Short-circuit current				±75		mA
C_{LOAD}	Capacitive load drive				1000		pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			525		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_{CM} = V–, I_O = 0 A			560	685	µA
			T_A = – -55°C to 125°C			750	

(1) Third-order filter; bandwidth = 80 kHz at – 3 dB.
(2) Specified by characterization only.

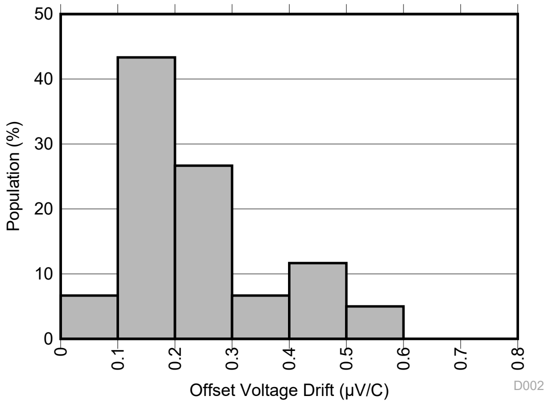
6.6 Typical Characteristics

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



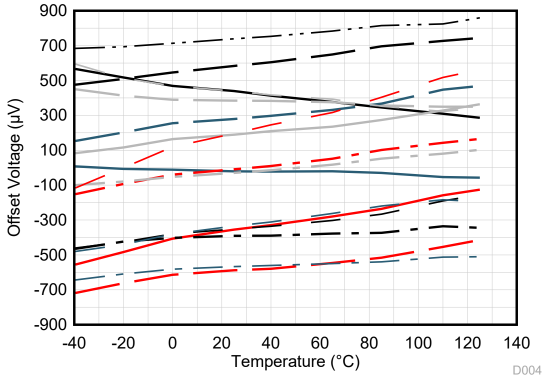
Distribution from 15462 amplifiers, T_A = 25°C

图 6-1. Offset Voltage Production Distribution



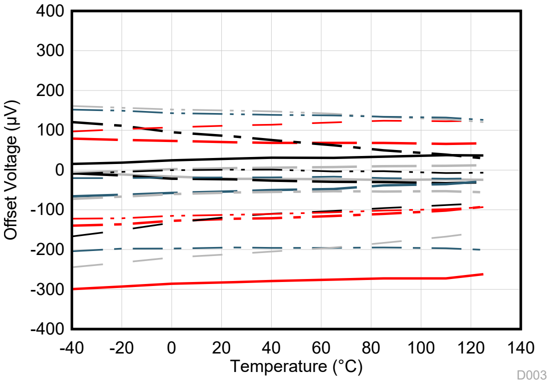
Distribution from 60 amplifiers

图 6-2. Offset Voltage Drift Distribution



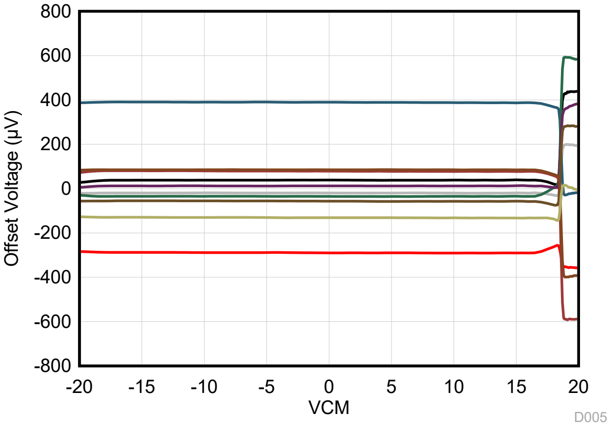
V_{CM} = V+

图 6-3. Offset Voltage vs Temperature



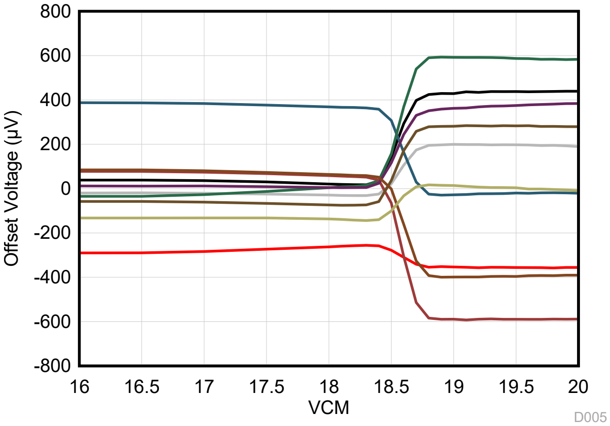
V_{CM} = V–

图 6-4. Offset Voltage vs Temperature



T_A = 25°C

图 6-5. Offset Voltage vs Common-Mode Voltage

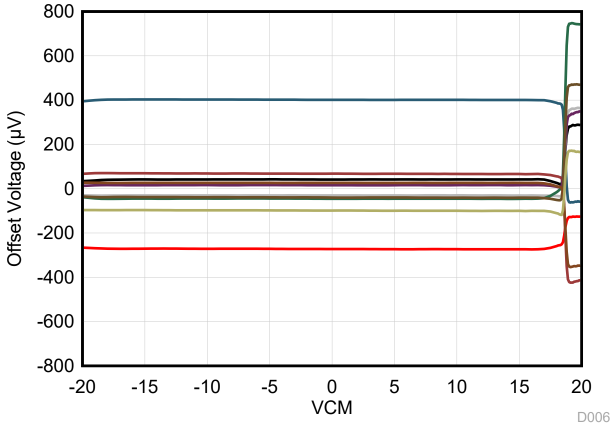


T_A = 25°C

图 6-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

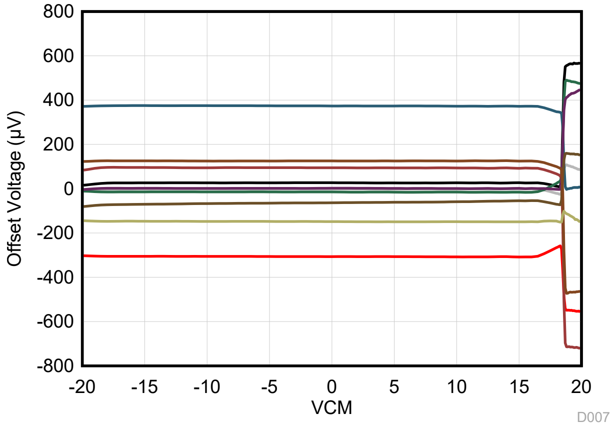
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



T_A = 125°C

图 6-7. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

图 6-8. Offset Voltage vs Common-Mode Voltage

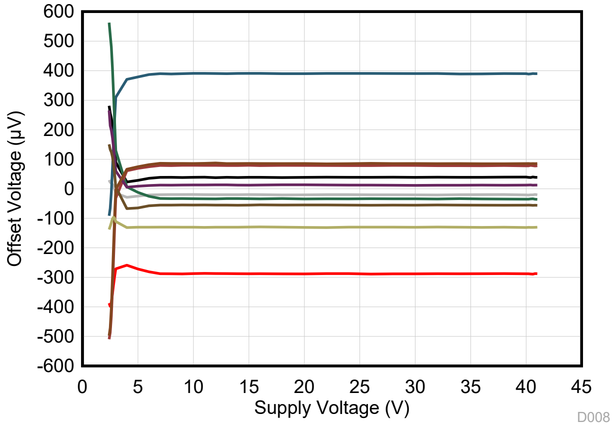
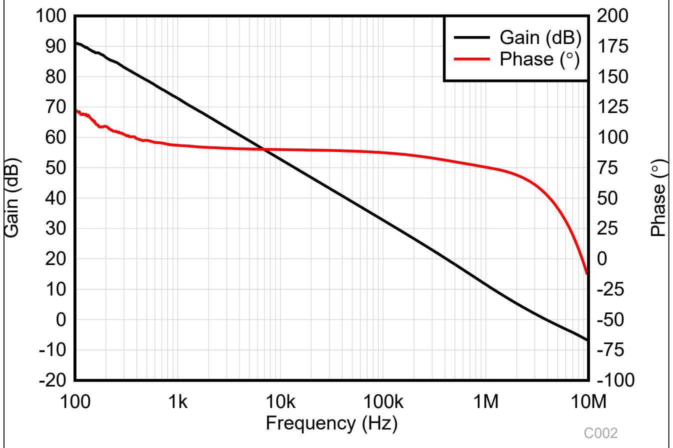


图 6-9. Offset Voltage vs Power Supply



C_L = 20 pF

图 6-10. Open-Loop Gain and Phase vs Frequency

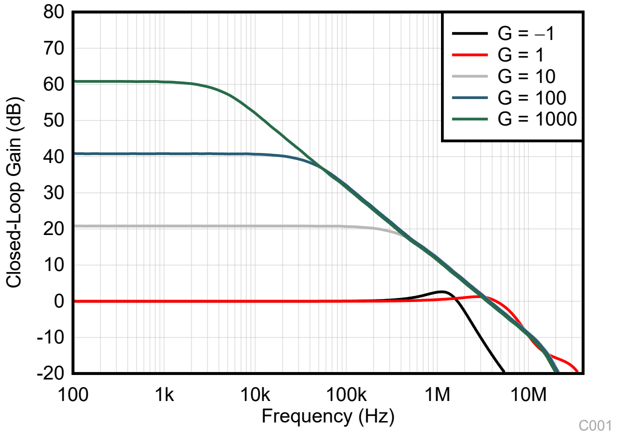


图 6-11. Closed-Loop Gain vs Frequency

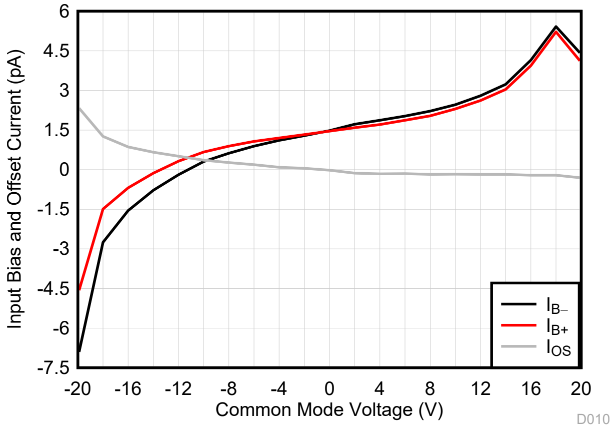


图 6-12. Input Bias Current vs Common-Mode Voltage

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)

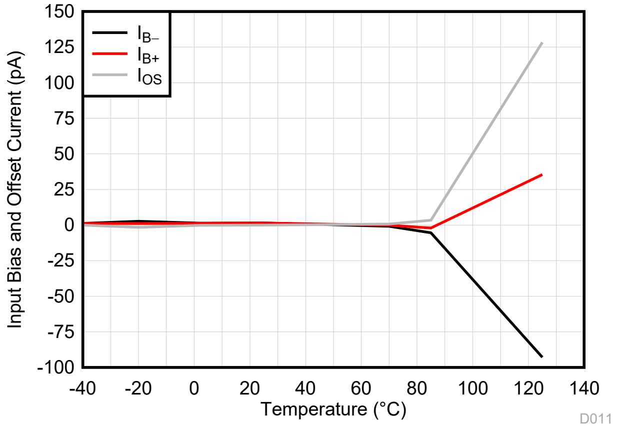


图 6-13. Input Bias Current vs Temperature

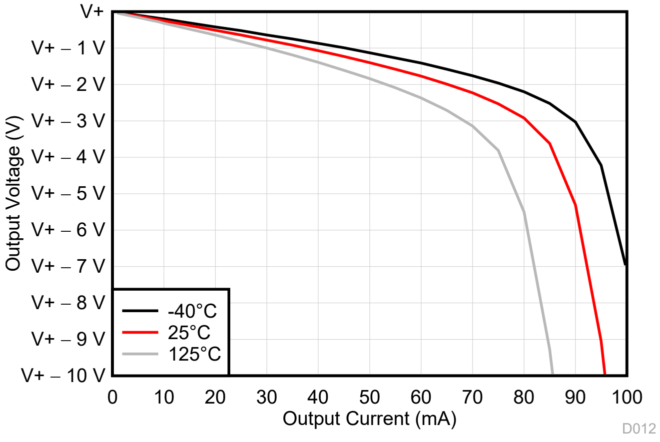


图 6-14. Output Voltage Swing vs Output Current (Sourcing)

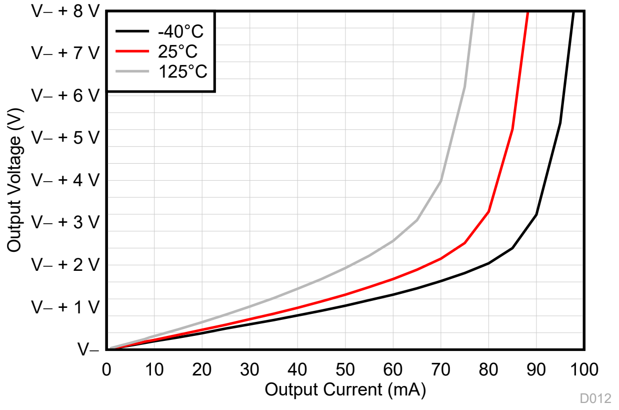


图 6-15. Output Voltage Swing vs Output Current (Sinking)

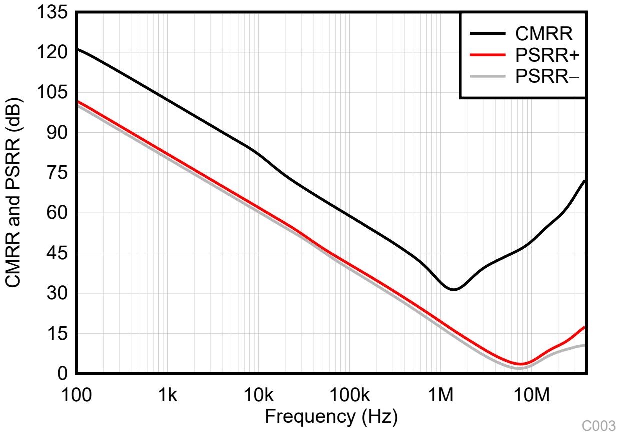
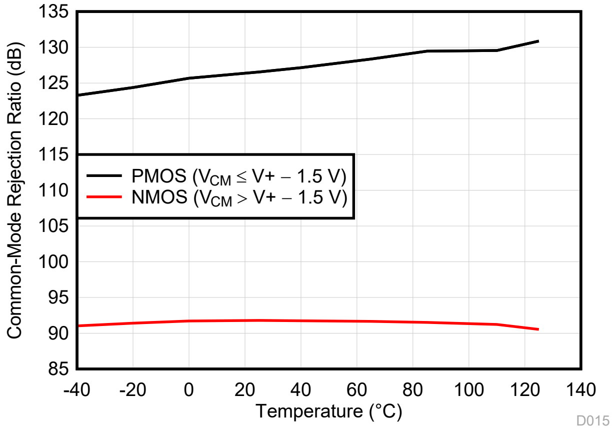
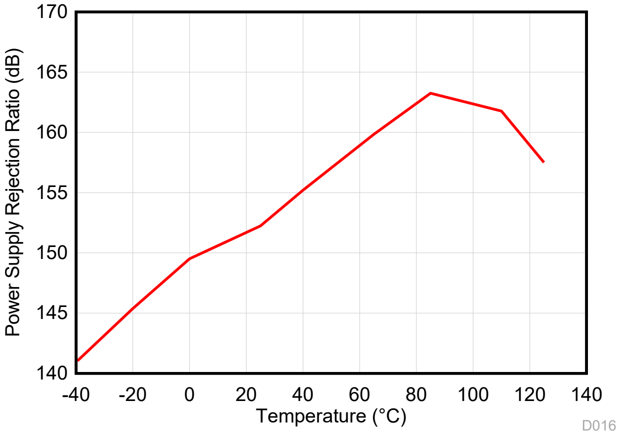


图 6-16. CMRR and PSRR vs Frequency



f = 0 Hz

图 6-17. CMRR vs Temperature (dB)



f = 0 Hz

图 6-18. PSRR vs Temperature (dB)

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)

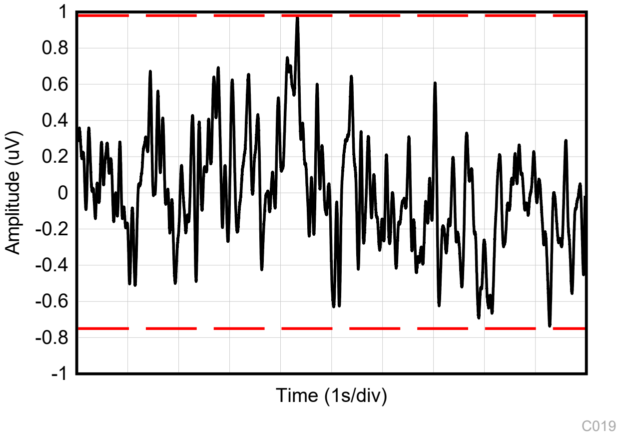


图 6-19. 0.1-Hz to 10-Hz Noise

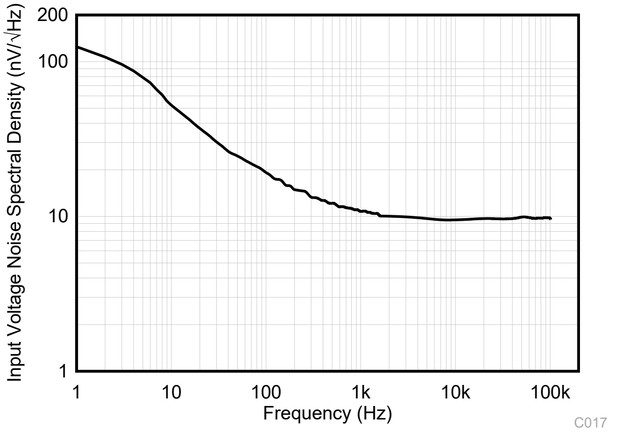
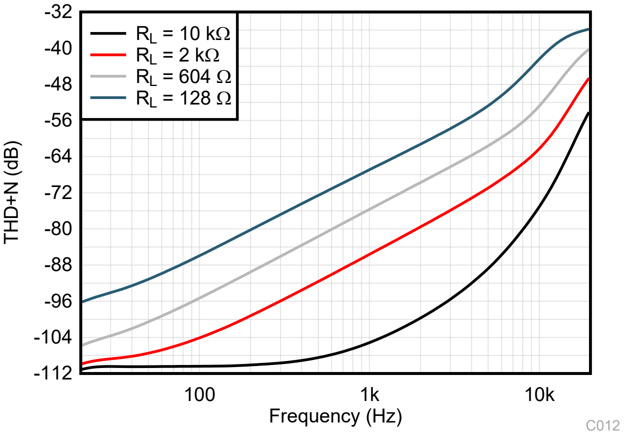
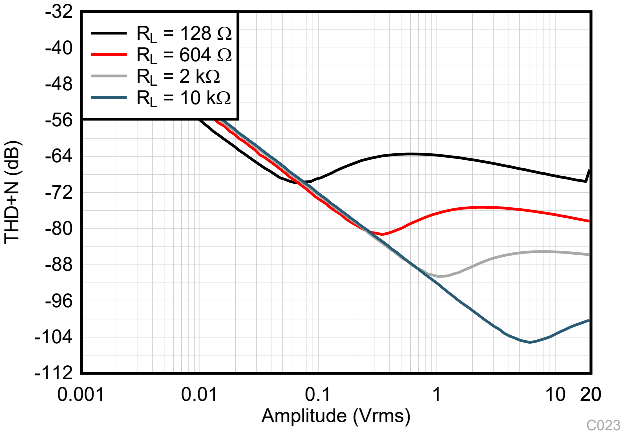


图 6-20. Input Voltage Noise Spectral Density vs Frequency



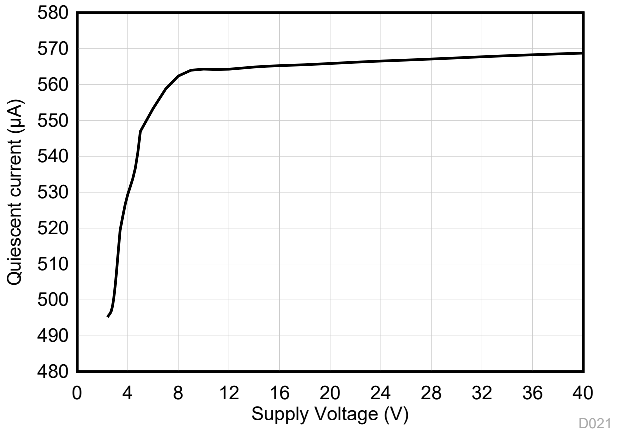
BW = 80 kHz, V_{OUT} = 1 V_{RMS}

图 6-21. THD+N Ratio vs Frequency



BW = 80 kHz, f = 1 kHz

图 6-22. THD+N vs Output Amplitude



V_{CM} = V –

图 6-23. Quiescent Current vs Supply Voltage

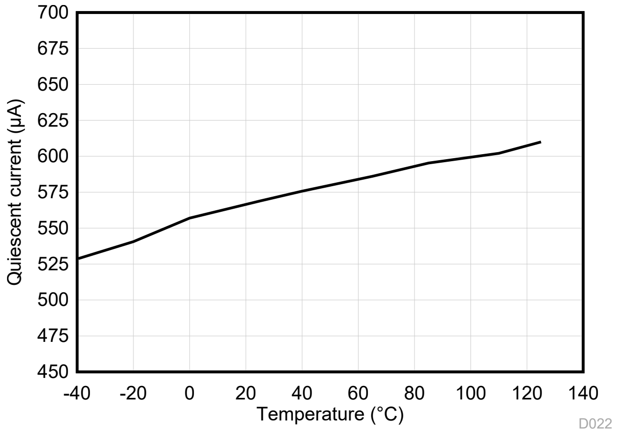


图 6-24. Quiescent Current vs Temperature

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)

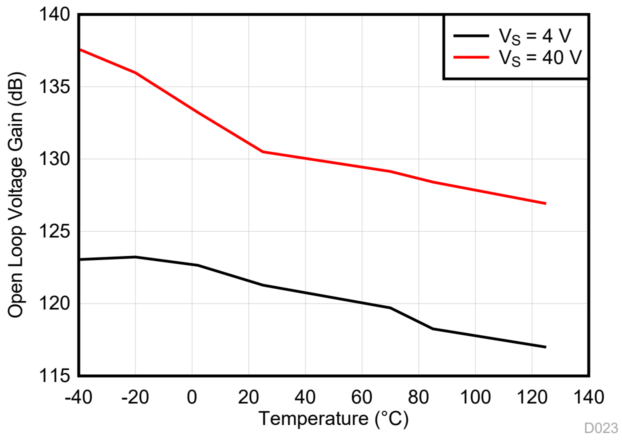


图 6-25. Open-Loop Voltage Gain vs Temperature (dB)

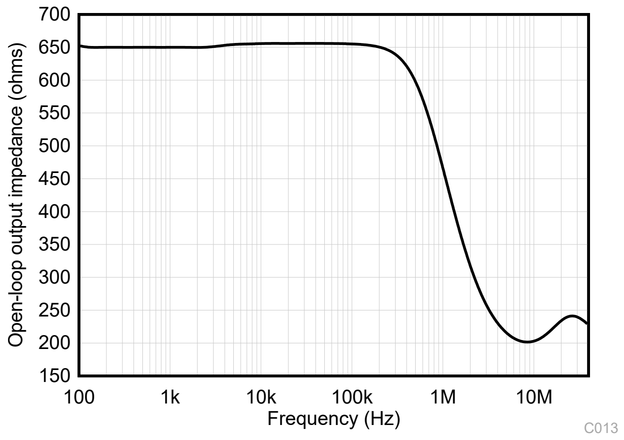
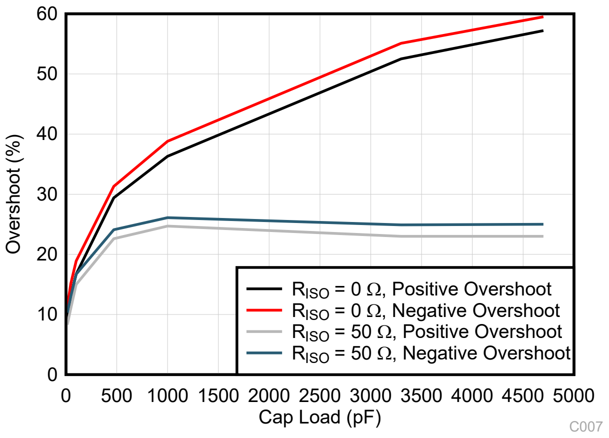
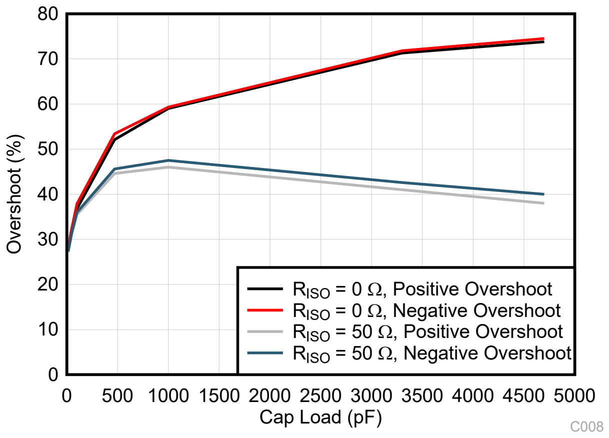


图 6-26. Open-Loop Output Impedance vs Frequency



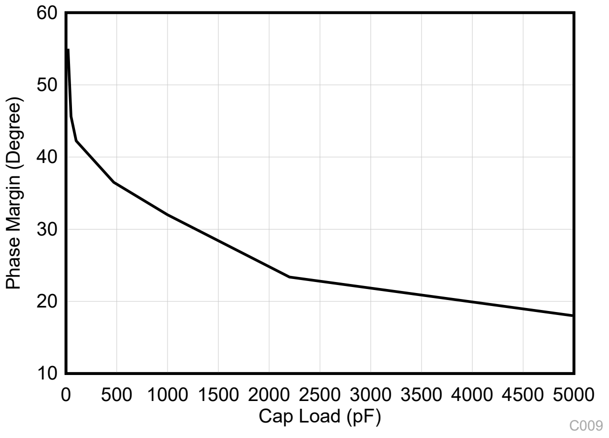
G = –1, 10-mV output step

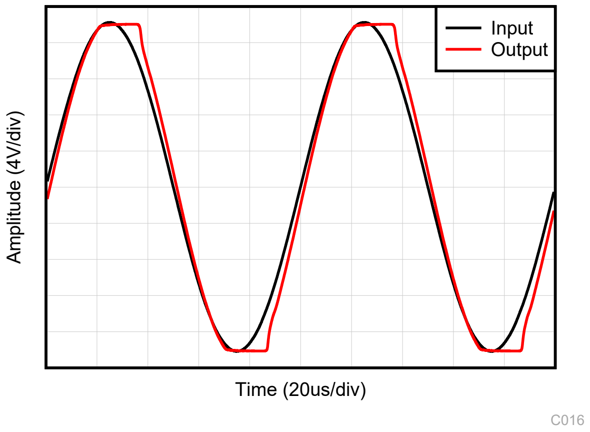
图 6-27. Small-Signal Overshoot vs Capacitive Load



G = 1, 10-mV output step

图 6-28. Small-Signal Overshoot vs Capacitive Load





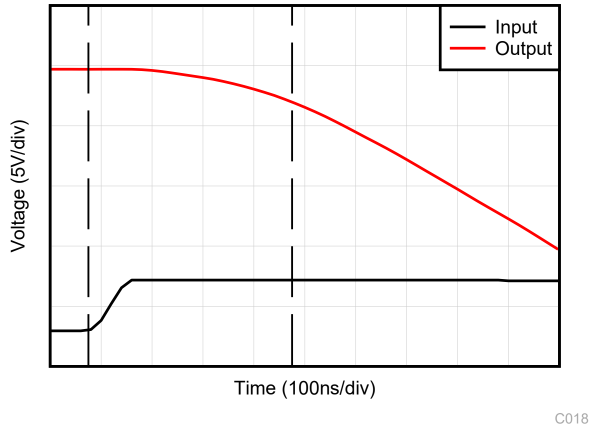
V_{IN} = ±20 V; V_S = V_{OUT} = ±17 V

图 6-29. Phase Margin vs Capacitive Load

图 6-30. No Phase Reversal

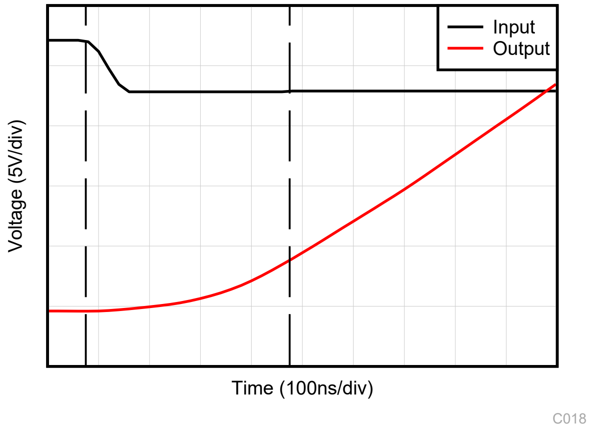
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



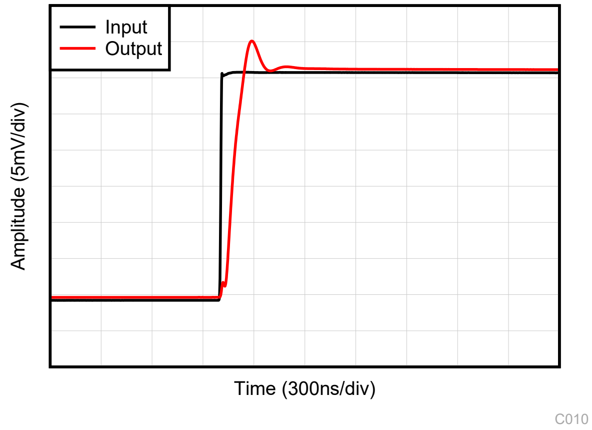
G = –10

图 6-31. Positive Overload Recovery



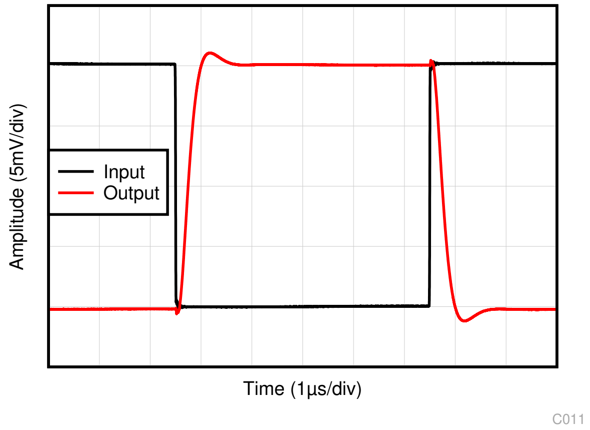
G = –10

图 6-32. Negative Overload Recovery



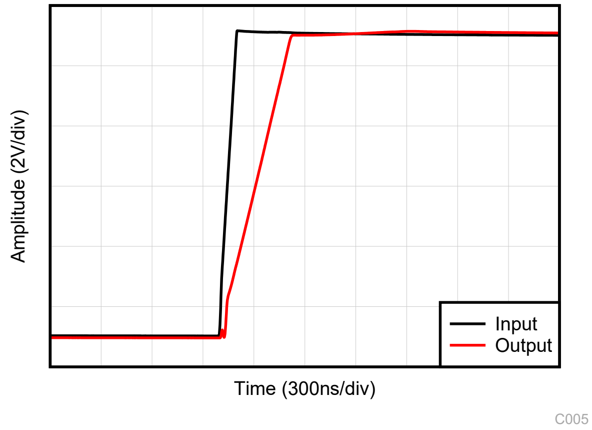
C_L = 20 pF, G = 1, 20-mV step response

图 6-33. Small-Signal Step Response, Rising



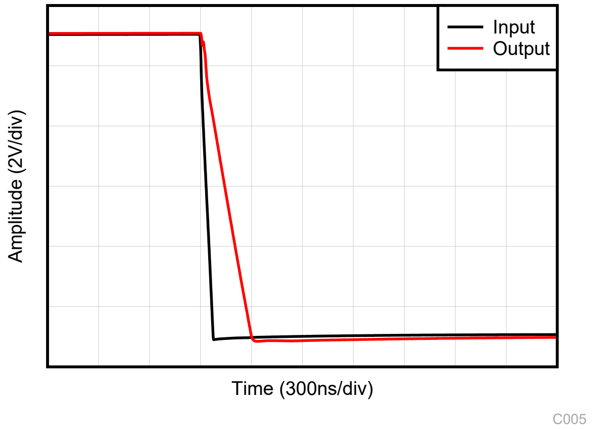
C_L = 20 pF, G = -1, 20-mV step response

图 6-34. Small-Signal Step Response



C_L = 20 pF, G = 1

图 6-35. Large-Signal Step Response (Rising)

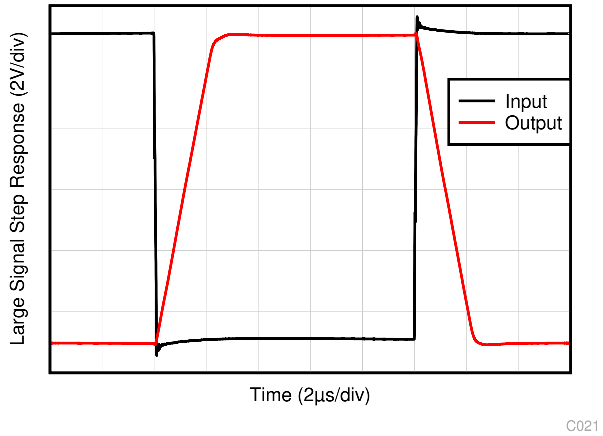


C_L = 20 pF, G = 1

图 6-36. Large-Signal Step Response (Falling)

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



C_L = 20 pF, G = −1

图 6-37. Large-Signal Step Response

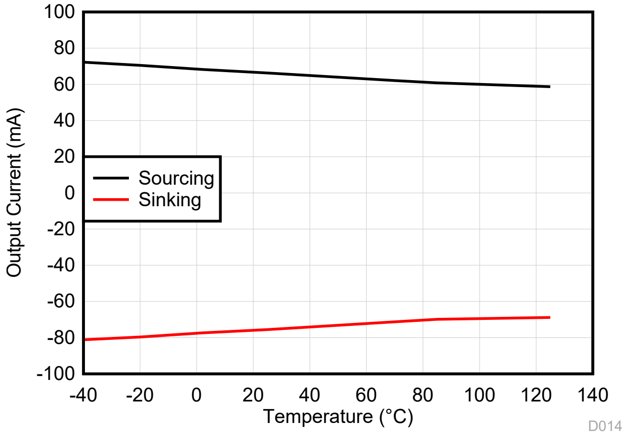


图 6-38. Short-Circuit Current vs Temperature

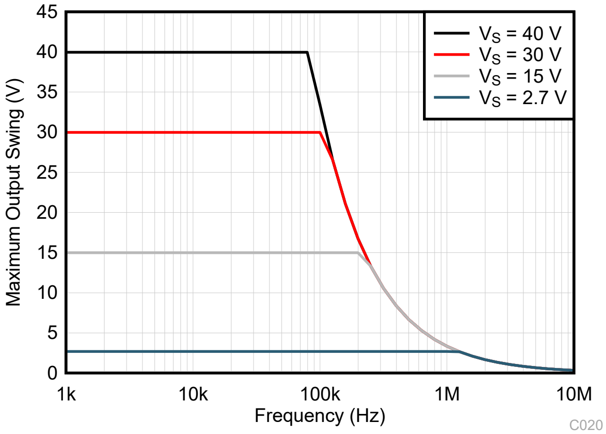


图 6-39. Maximum Output Voltage vs Frequency

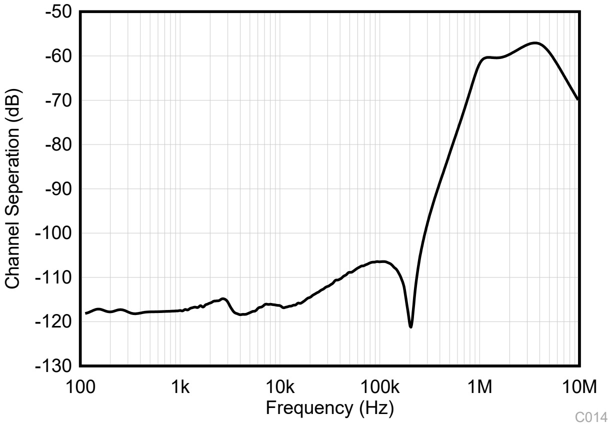


图 6-40. Channel Separation vs Frequency

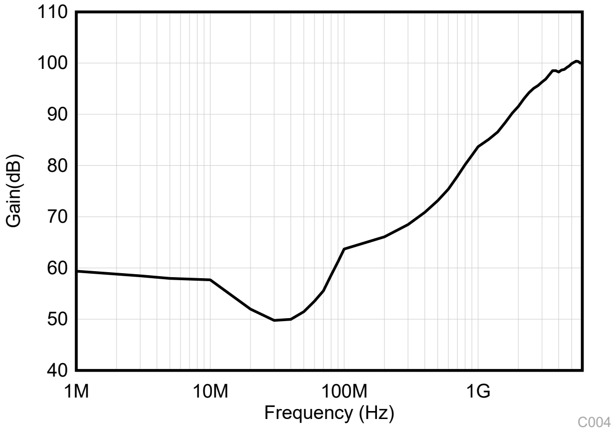


图 6-41. EMIRR (Electromagnetic Interference Rejection Ratio) at Inputs vs Frequency

7 Detailed Description

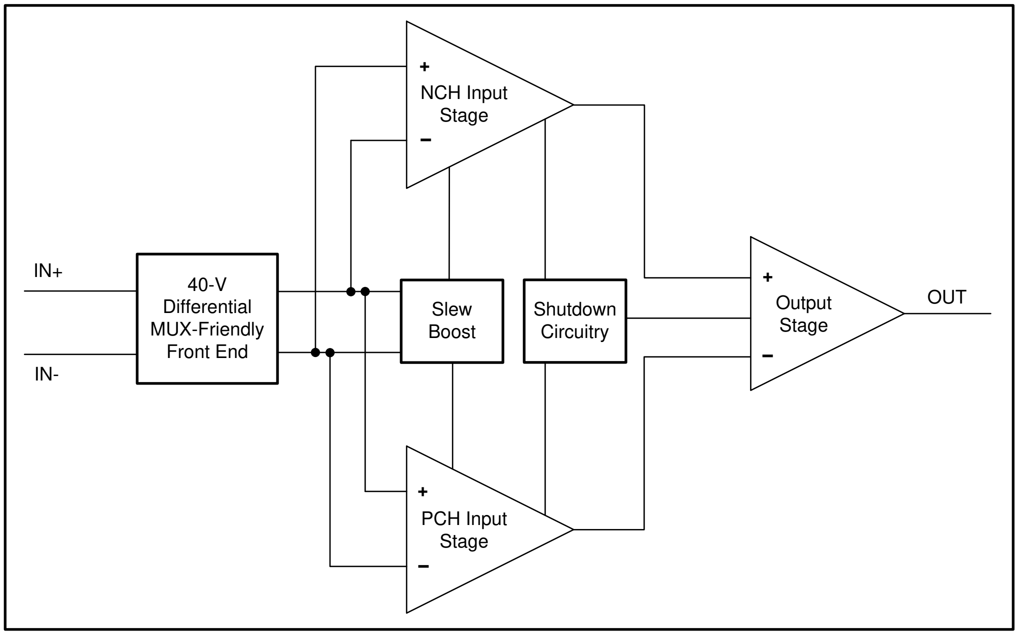
7.1 Overview

The OPA4991-EP is a new 40-V general purpose operational amplifier.

This device offers excellent DC precision and AC performance, including rail-to-rail input/output, low offset (±125 μV, typ), low offset drift (±0.3 μV/°C, typ), and 4.5-MHz bandwidth.

Unique features such as differential and common-mode input-voltage range to the supply rail, high output current (±75 mA) and high slew rate (21 V/μs) make the OPA4991-EP a robust, high-performance operational amplifier for high-voltage automotive applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Protection Circuitry

The OPA4991-EP uses a unique input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. 图 7-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in 图 7-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

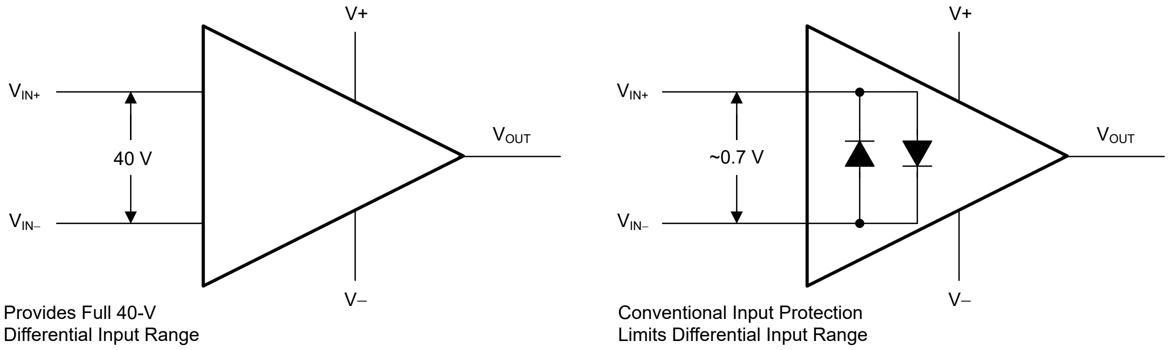
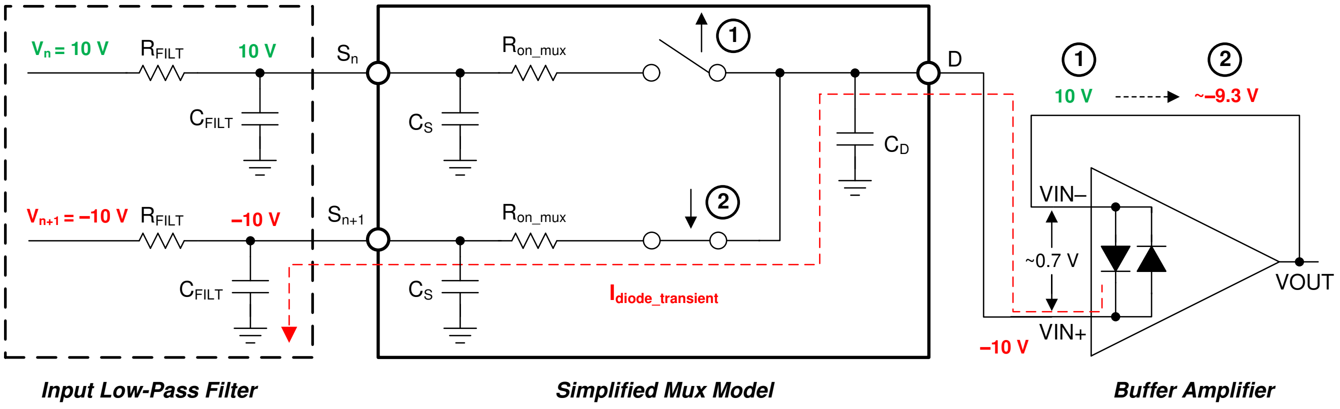


图 7-1. OPA4991-EP Input Protection Does Not Limit Differential Input Capability



Input Low-Pass Filter *Simplified Mux Model* *Buffer Amplifier*

图 7-2. Back-to-Back Diodes Create Settling Issues

The OPA4991-EP family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device designed for op amp for multichannel, high-switched, input applications. The OPA4991-EP tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 40 V, making the device an excellent choice for use as a comparator or in applications with fast-ramping input signals such as data-acquisition systems; see the TI TechNote *MUX-Friendly Precision Operational Amplifiers* for more information.

7.3.2 EMI Rejection

The OPA4991-EP uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPA4991-EP benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 7-3 shows the results of this testing on the OPA4991-EP. 表 7-1 shows the EMIRR IN+ values for the OPA4991-EP at particular frequencies commonly encountered in real-world applications. The *EMI Rejection*

Ratio of Operational Amplifiers application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

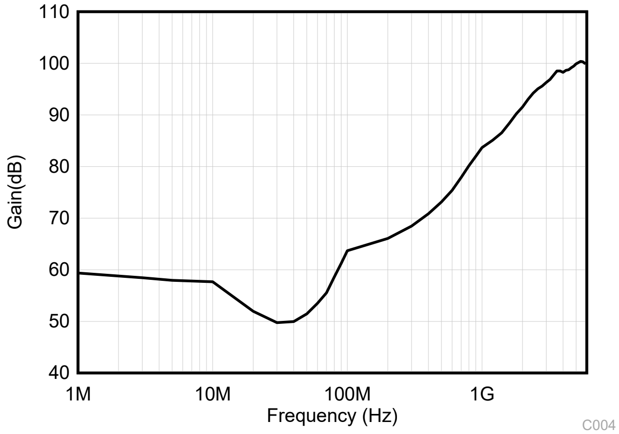


图 7-3. EMIRR Testing

表 7-1. OPA4991-EP EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	73.2 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	82.5 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	89.7 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	93.9 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	95.7 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	98.0 dB

7.3.3 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPA4991-EP is 150°C. Exceeding this temperature causes damage to the device. The OPA4991-EP has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. 图 7-4 shows an application example for the OPA4991-EP that has significant self heating because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C, the device junction temperature will reach 177°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. 图 7-4 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L. If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected.

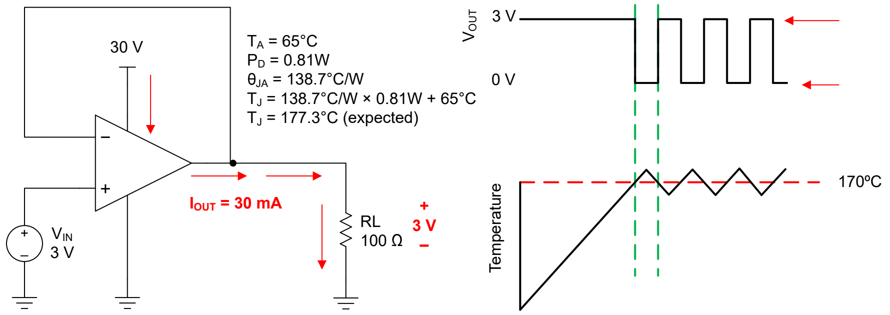


图 7-4. Thermal Protection

If the device continues to operate at high junction temperatures with high output power over a long period of time, regardless if the device is or is not entering thermal shutdown, the thermal dissipation of the device can slowly degrade performance of the device and eventually cause catastrophic destruction. Designers should be careful to limit output power of the device at high temperatures, or control ambient and junction temperatures under high output power conditions.

7.3.4 Capacitive Load and Stability

The OPA4991-EP features a resistive output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 图 7-5 and 图 7-6. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

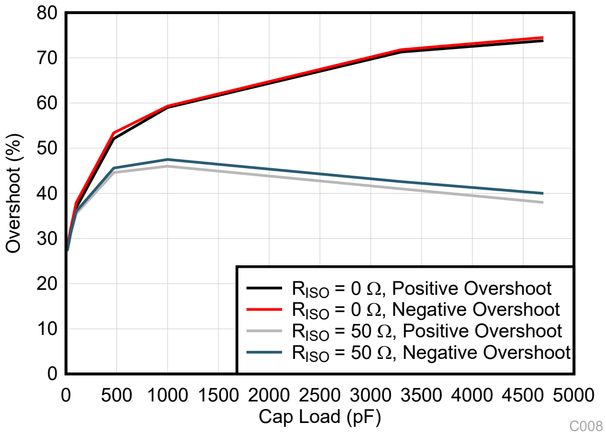


图 7-5. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = 1)

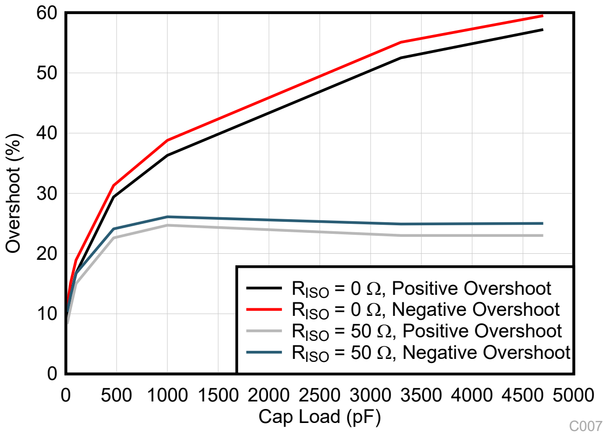


图 7-6. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = – 1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO}, in series with the output, as shown in 图 7-7. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPA4991-EP an excellent choice for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 图 7-7 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

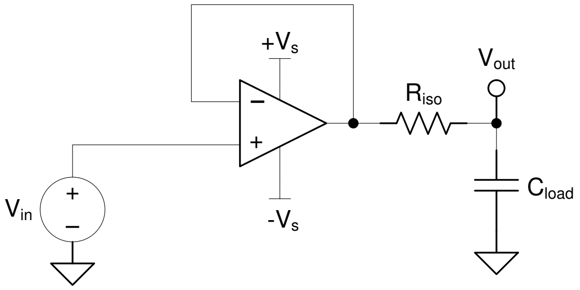


图 7-7. Extending Capacitive Load Drive With the OPA4991-EP

7.3.5 Common-Mode Voltage Range

The OPA4991-EP is a 40-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in 图 7-8. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 2 V. There is a small transition region, typically (V+) – 2 V to (V+) – 1 V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

图 6-5 shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.

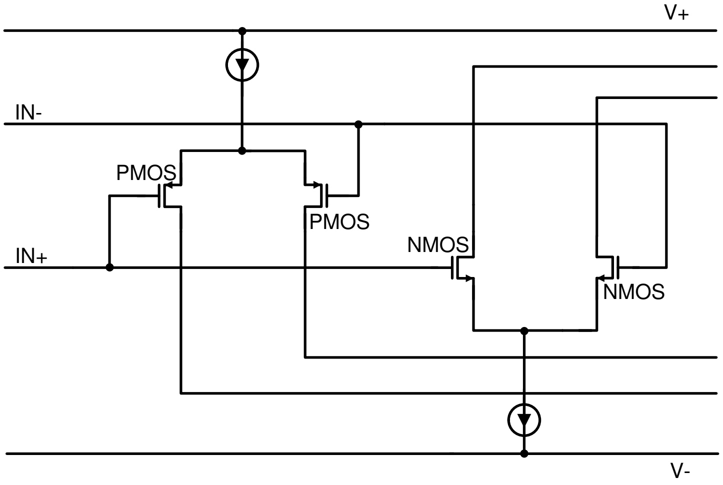


图 7-8. Rail-to-Rail Input Stage

7.3.6 Phase Reversal Protection

The OPA4991-EP family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPA4991-EP is a rail-to-rail input op amp; therefore, the common-mode range can extend beyond the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in 图 7-9. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.

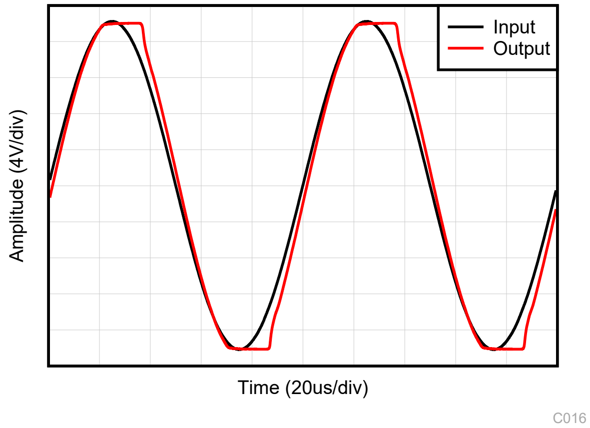


图 7-9. No Phase Reversal

7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 7-10 shows an illustration of the ESD circuits contained in the OPA4991-EP (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

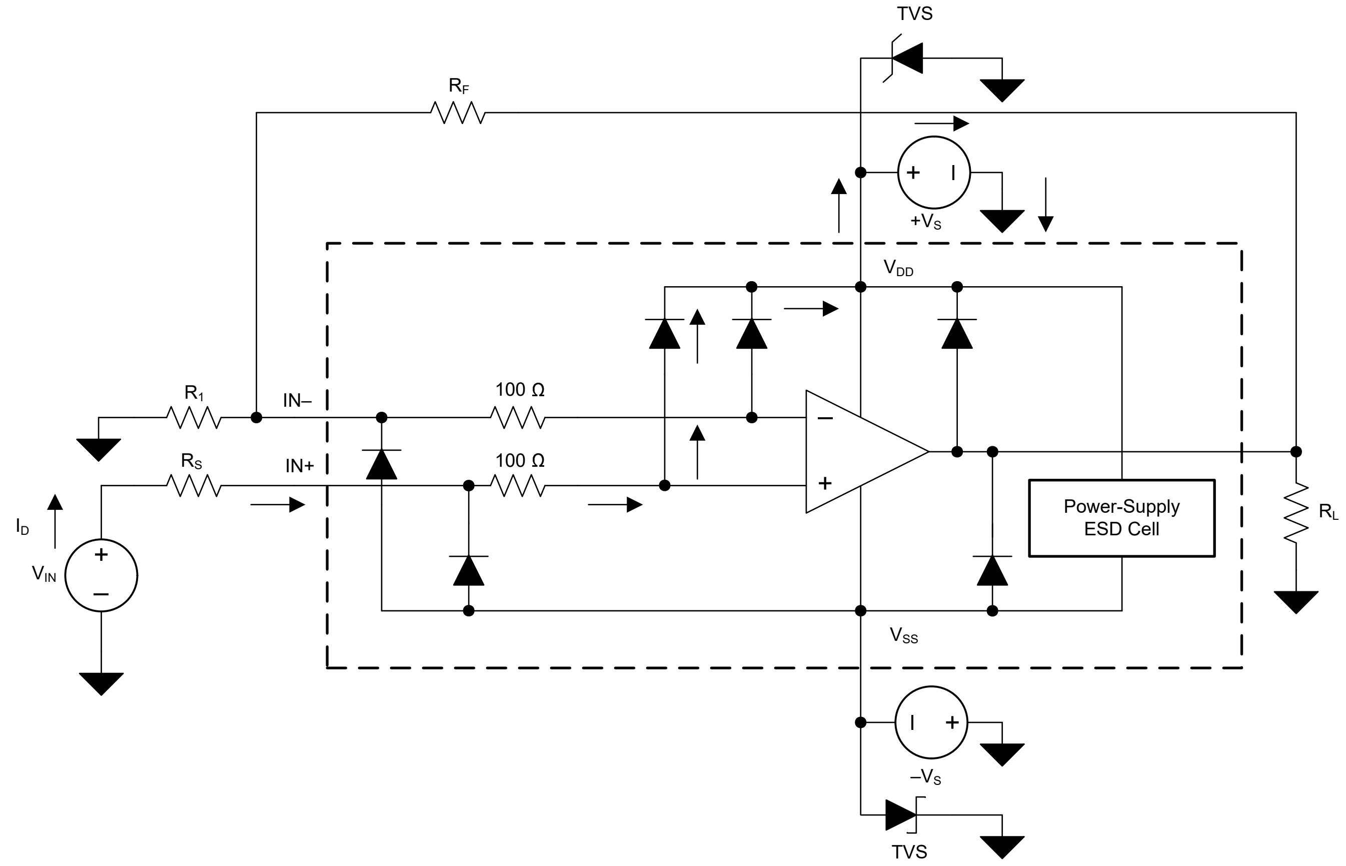


图 7-10. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example; 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example; 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

7.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPA4991-EP is approximately 400 ns.

7.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier can exhibit some amount of deviation from the preferred value, like the input offset voltage of the amplifier. These deviations often follow *Gaussian* (bell curve), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the 节 *6.5*.

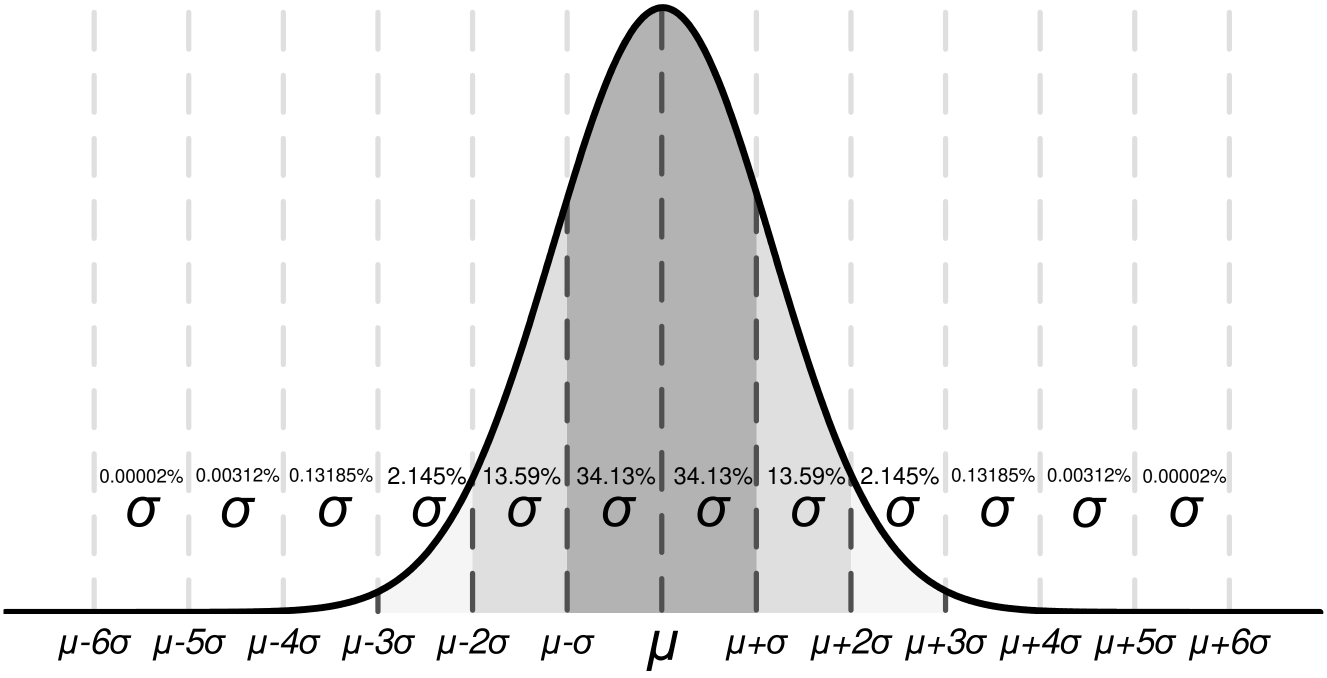


图 7-11. Ideal Gaussian Distribution

图 7-11 shows an example distribution, where μ, or *mu*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of the 节 *6.5* table are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for OPA4991-EP, the typical input voltage offset is 125 µV, so 68.2% of all OPA4991-EP devices are expected to have an offset from –125 µV to 125 µV. At 4 σ (±500 µV), 99.9937% of the distribution has an offset voltage less than

±500 µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are specified by TI, and units outside these limits will be removed from production material. For example, the OPA4991-EP family has a maximum offset voltage of 895 µV at 25°C, and even though this corresponds to more than 5 σ (≈1 in 1.7 million units), which is extremely unlikely, any unit with larger offset than 895 µV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6-σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and can be an option as a wide guardband to design a system around. In this case, the OPA4991-EP family does not have a maximum or minimum for offset voltage drift, but based on 图 6-2 and the typical value of 0.3 µV/°C in the *节 6.5*, the 6-σ value for offset voltage drift is about 1.8 µV/°C when calculated. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot be sure of the performance of a device. This information must be used only to estimate the performance of a device.

7.4 Device Functional Modes

The OPA4991-EP has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V (±1.35 V). The maximum power supply voltage for the OPA4991-EP is 40 V (±20 V).

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPA4991-EP family offers excellent DC precision and AC performance. These devices operate up to 40-V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 4.5-MHz bandwidth and high output drive. These features make the OPA4991-EP a robust, high-performance operational amplifier for high-voltage industrial applications.

8.2 Typical Applications

8.2.1 Low-Side Current Measurement

图 8-1 shows the OPA4991-EP configured in a low-side current sensing application. For a full analysis of the circuit shown in 图 8-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0-A to 1-A Single-Supply Low-Side Current-Sensing Solution*.

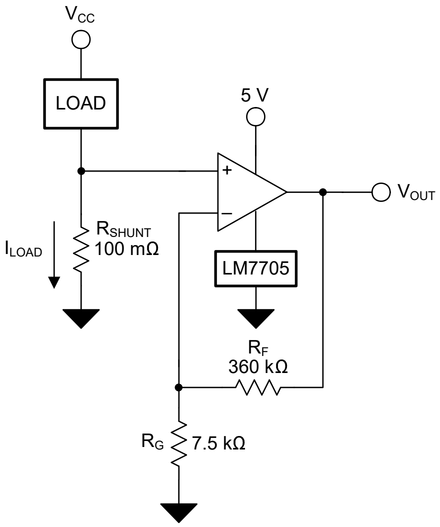


图 8-1. OPA4991-EP in a Low-Side, Current-Sensing Application

8.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

8.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 图 8-1 is given in 方程式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using 方程式 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \tag{2}$$

Using 方程式 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPA4991-EP to produce an output voltage of 0 V to 4.9 V. The gain needed by the OPA4991-EP to produce the necessary output voltage is calculated using 方程式 3.

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \tag{3}$$

Using 方程式 3, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. 方程式 4 is used to size the resistors, R_F and R_G, to set the gain of the OPA4991-EP to 49 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \tag{4}$$

Choosing R_F as 360 kΩ, R_G is calculated to be 7.5 kΩ. R_F and R_G were chosen as 360 kΩ and 7.5 kΩ because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. 图 8-2 shows the measured transfer function of the circuit shown in 图 8-1.

8.2.1.3 Application Curve

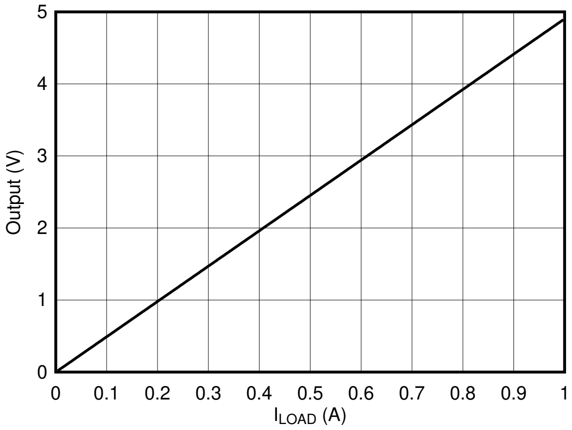


图 8-2. Low-Side, Current-Sense, Transfer Function

8.3 Power Supply Recommendations

The OPA4991-EP is specified for operation from 2.7 V to 40 V (±1.35 V to ±40 V); many specifications apply from – 55°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to *Layout*.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 图 8-4, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

8.4.2 Layout Example

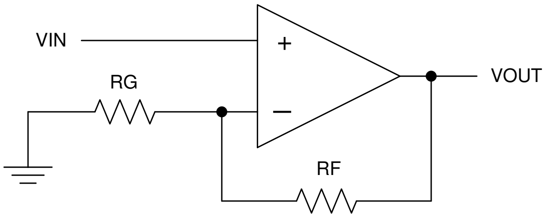


图 8-3. Schematic Representation

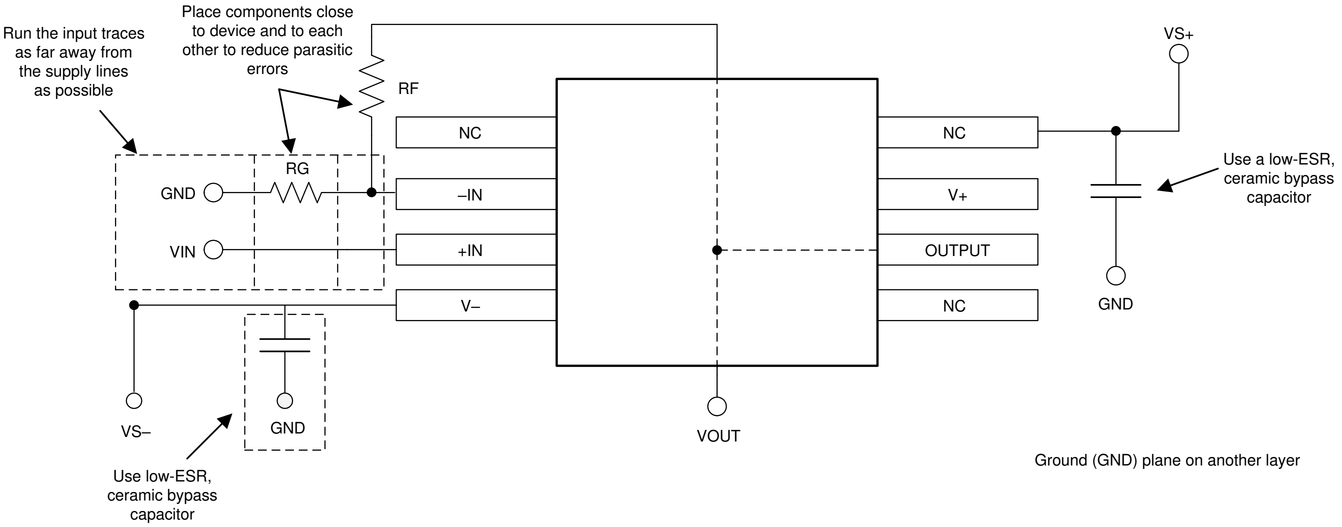


图 8-4. Operational Amplifier Board Layout for Noninverting Configuration

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

备注

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Analog Engineer's Circuit Cookbook: Amplifiers* solution guide

Texas Instruments, *AN31 Amplifier Circuit Collection* application note

Texas Instruments, *MUX-Friendly Precision Operational Amplifiers* application brief

Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report

Texas Instruments, *Op Amps With Complementary-Pair Input Stages* application note

9.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4991MDYYREP	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	OPA4991EP	Samples
V62/21615-01XE	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	OPA4991EP	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA4991-EP :

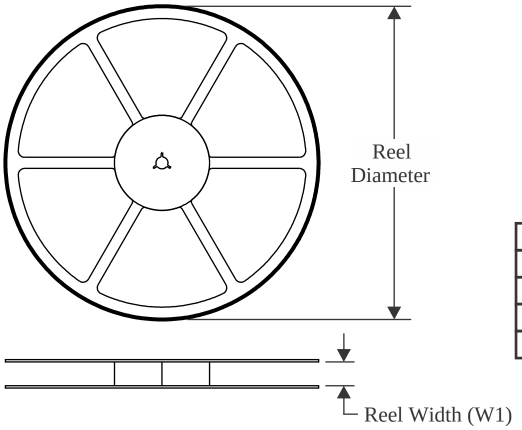
- Catalog : OPA4991
- Automotive : OPA4991-Q1

NOTE: Qualified Version Definitions:

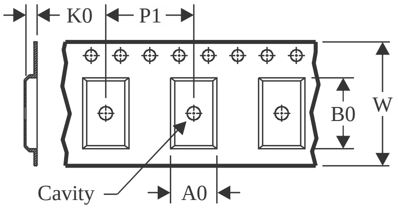
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

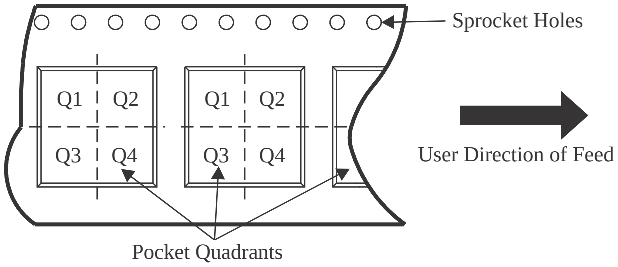


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

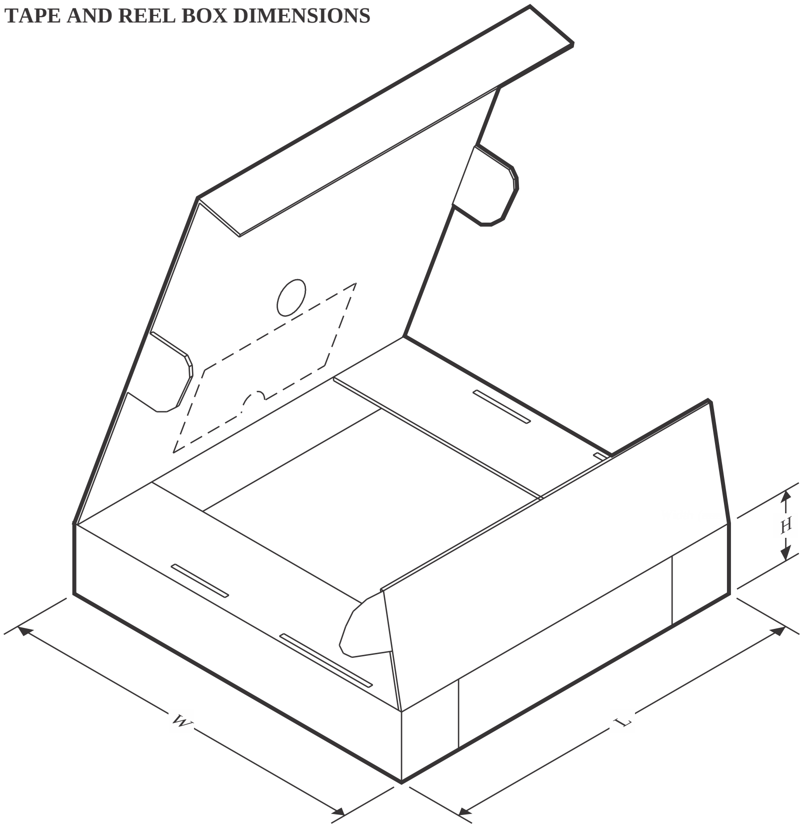
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4991MDYYREP	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

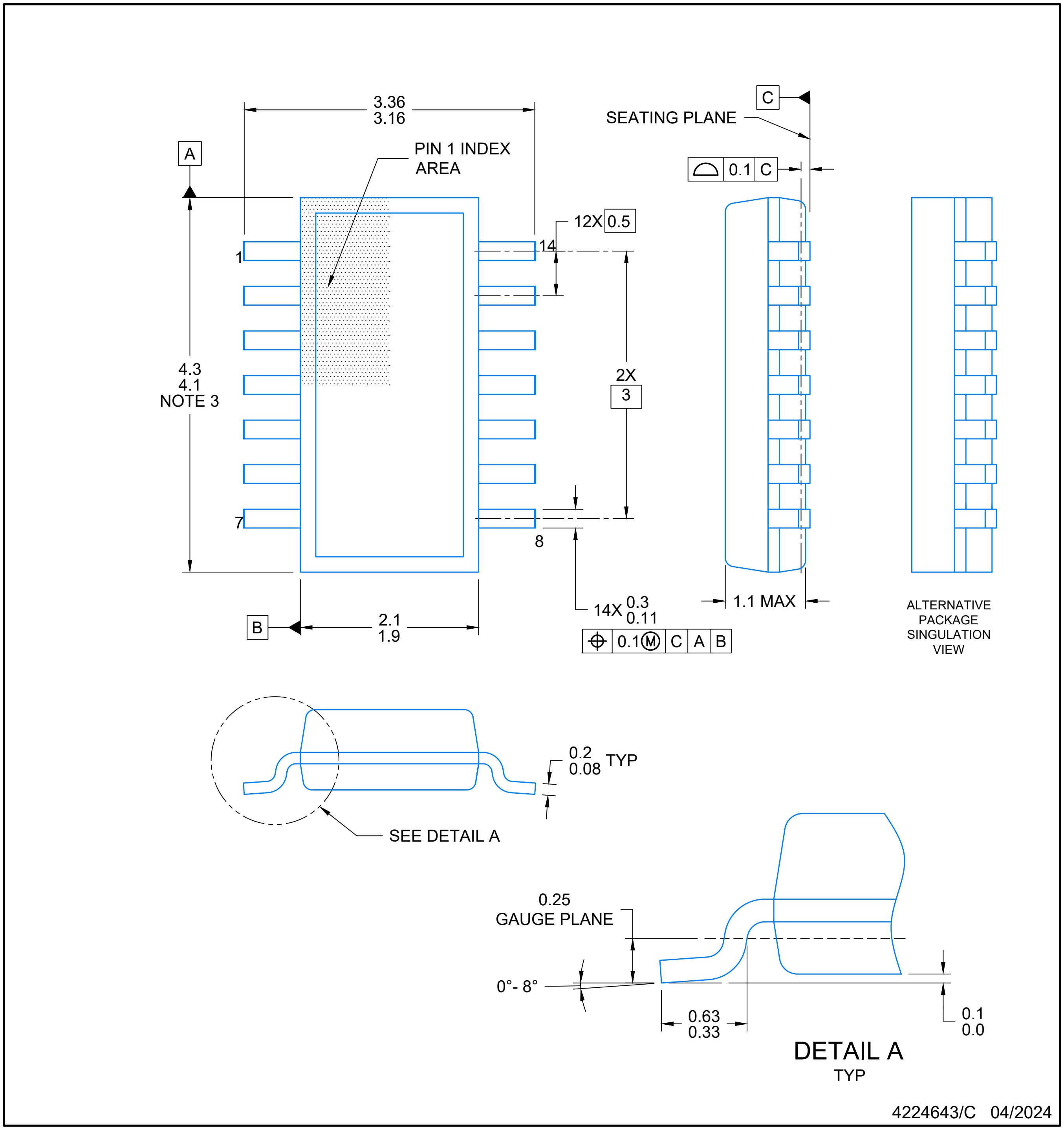
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4991MDYYREP	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8

PACKAGE OUTLINE

DYY0014A

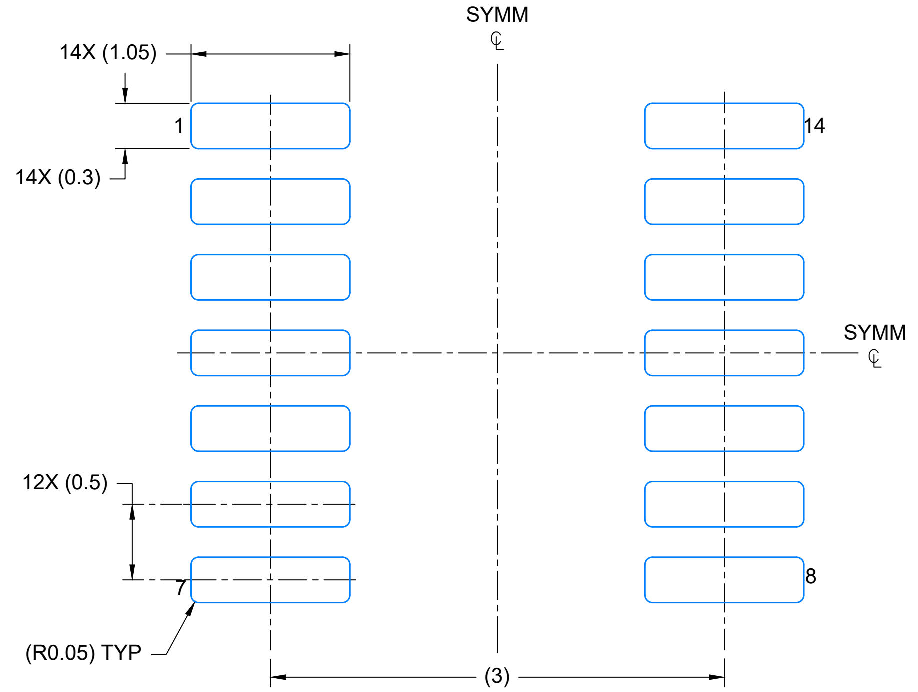
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

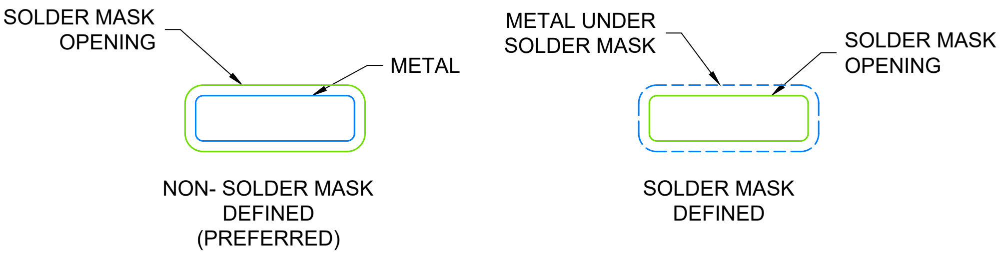


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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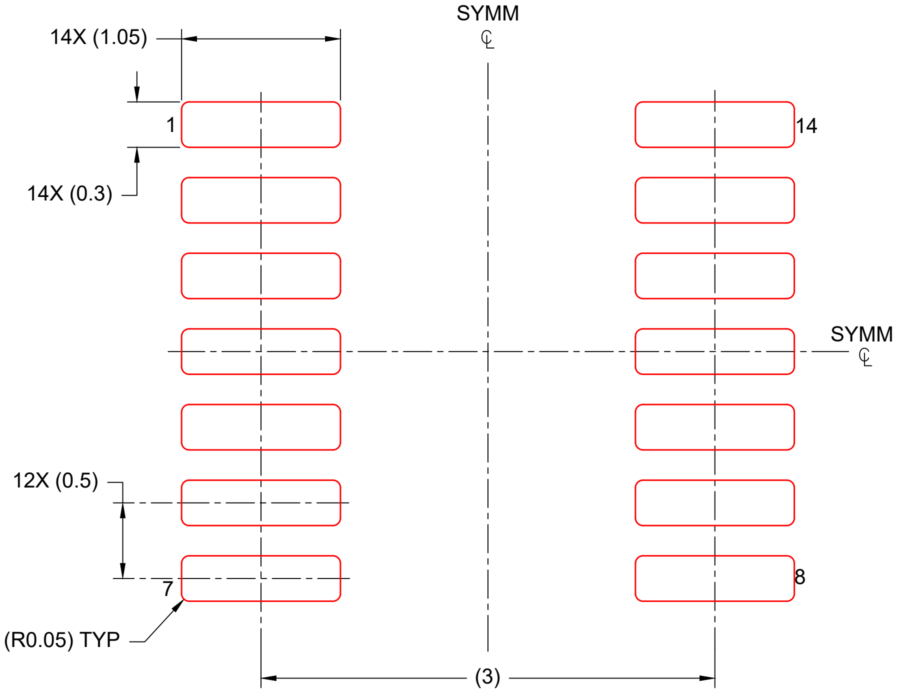
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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