

## High Survivability, Low Noise Amplifier, 1 GHz to 20 GHz

### FEATURES

- ▶ High RF input power survivability: 32 dBm
- ▶ Integrated AC coupling capacitors and bias inductor
- ▶ Single positive supply: 5 V with  $I_{DQ} = 175$  mA
- ▶ RBIAS drain current adjustment pin
- ▶ Gain: 13 dB typical from 2 GHz to 18 GHz
- ▶ OIP3: 28 dBm typical from 2 GHz to 18 GHz
- ▶ OIP2: 48 dBm typical from 2 GHz to 18 GHz

### APPLICATIONS

- ▶ Electronic warfare
- ▶ Test and measurement equipment
- ▶ Satellite communications

### GENERAL DESCRIPTION

The ADL7078 is a 1 GHz to 20 GHz low noise amplifier (LNA) with 32 dBm RF input power survivability. AC-coupling capacitors and bias inductors are integrated, facilitating a compact printed circuit board (PCB) footprint.

The ADL7078 has a gain of 13 dB, an output power for 1 dB compression (OP1dB) of 16.5 dBm, a typical output third-order intercept (OIP3) of 28 dBm, and a noise figure of 4.4 dB from 2

### FUNCTIONAL BLOCK DIAGRAM

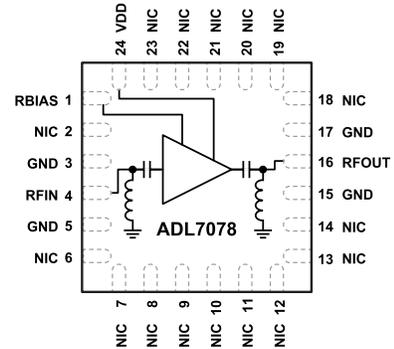


Figure 1. Functional Block Diagram

GHz to 18 GHz. This LNA operates on a 5 V supply voltage ( $V_{DD}$ ) and has a nominal quiescent current ( $I_{DQ}$ ) of 175 mA.

The ADL7078 is fabricated on a gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT) process. This device is housed in a [RoHS-compliant, 24-lead, 4.00 mm × 4.00 mm, lead frame chip scale package \[LFCS\]](#) and is specified for operation from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

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**REVISION HISTORY****10/2023—Revision 0: Initial Version**

## SPECIFICATIONS

## 1 GHz TO 2 GHz FREQUENCY RANGE

Supply voltage ( $V_{DD}$ ) = 5 V, quiescent current ( $I_{DQ}$ ) = 175 mA, bias resistance ( $R_{BIAS}$ ) = 698  $\Omega$ , and  $T_{CASE}$  = 25°C, unless otherwise noted.

Table 1. 1 GHz to 2 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	1		2	GHz	
GAIN (S21)		11		dB	
Gain Variation over Temperature		0.043		dB/°C	
NOISE FIGURE		5		dB	
RETURN LOSS					
Input (S11)		9.5		dB	
Output (S22)		12.5		dB	
OUTPUT					
OP1dB		16		dBm	
Saturated Power ( $P_{SAT}$ )		19		dBm	
OIP3		27.5		dBm	Measurement taken at output power ( $P_{OUT}$ ) per tone = 0 dBm
Second-Order Intercept (OIP2)		45		dBm	Measurement taken at $P_{OUT}$ per tone = 0 dBm
POWER ADDED EFFICIENCY (PAE)		6.7		%	Measured at $P_{SAT}$

## 2 GHz TO 18 GHz FREQUENCY RANGE

$V_{DD}$  = 5 V,  $I_{DQ}$  = 175 mA,  $R_{BIAS}$  = 698  $\Omega$ , and  $T_{CASE}$  = 25°C, unless otherwise noted.

Table 2. 2 GHz to 18 GHz Frequency Range Specification

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	2		18	GHz	
S21	11	13		dB	
Gain Variation over Temperature		0.032		dB/°C	
NOISE FIGURE		4.4		dB	
RETURN LOSS					
S11		17		dB	
S22		16		dB	
OUTPUT					
OP1dB	13.5	16.5		dBm	
$P_{SAT}$		18.5		dBm	
OIP3		28		dBm	Measurement taken at $P_{OUT}$ per tone = 0 dBm
OIP2		48		dBm	Measurement taken at $P_{OUT}$ per tone = 0 dBm
PAE		7.6		%	Measured at $P_{SAT}$

## SPECIFICATIONS

## 18 GHz TO 20 GHz FREQUENCY RANGE

$V_{DD} = 5\text{ V}$ ,  $I_{DQ} = 175\text{ mA}$ ,  $R_{BIAS} = 698\ \Omega$ , and  $T_{CASE} = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3. 18 GHz to 20 GHz Frequency Range Specification**

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	18		20	GHz	
S21		12		dB	
Gain Variation over Temperature		0.053		dB/°C	
NOISE FIGURE		6.5		dB	
RETURN LOSS					
S11		17.5		dB	
S22		16		dB	
OUTPUT					
OP1dB		8.5		dBm	
$P_{SAT}$		12.5		dBm	
OIP3		23.5		dBm	Measurement taken at $P_{OUT}$ per tone = 0 dBm
OIP2		47		dBm	Measurement taken at $P_{OUT}$ per tone = 0 dBm
PAE		4.3		%	Measured at $P_{SAT}$

## DC SPECIFICATIONS

$R_{BIAS} = 698\ \Omega$ , and  $T_{CASE} = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4. DC Specification**

Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT				
$I_{DQ}$		175		mA
Amplifier Current ( $I_{DQ\_AMP}$ )		170.5		mA
RBIAS Current ( $I_{RBIAS}$ )		4.5		mA
SUPPLY VOLTAGE				
$V_{DD}$	4.75	5	5.25	V

## ABSOLUTE MAXIMUM RATINGS

**Table 5. Absolute Maximum Ratings**

Parameter	Rating
$V_{DD}$	7 V
RF Input Power Survivability (RFIN)	32 dBm
Pulsed RFIN Power (Duty Cycle = 10%, Pulse Width = 100 $\mu$ s)	34 dBm
Continuous Power Dissipation ( $P_{DISS}$ ), $T_{CASE} = 85^{\circ}\text{C}$ (Derate 28.7 mW/ $^{\circ}\text{C}$ Above 85 $^{\circ}\text{C}$ )	2.57 W
Temperature	
Storage Range	-65 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$
Operating Range	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$
Quiescent Channel ( $T_{CASE} = 85^{\circ}\text{C}$ , $V_{DD} = 5\text{ V}$ , $I_{DQ} = 175\text{ mA}$ , Input Power ( $P_{IN}$ ) = Off)	115.63 $^{\circ}\text{C}$
Maximum Channel	175 $^{\circ}\text{C}$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

$\theta_{JC}$  is the channel-to-case thermal resistance (channel to exposed metal ground paddle on the underside of the device).

**Table 6. Thermal Resistance<sup>1</sup>**

Package Type	$\theta_{JC}$	Unit
CP-24-15		
Worst Case <sup>2</sup>	35	$^{\circ}\text{C}/\text{W}$

<sup>1</sup> Thermal Resistance varies with operating conditions.

<sup>2</sup> Worst case across all specified operating conditions,  $T_{CASE} = 85^{\circ}\text{C}$ .

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

### ESD Ratings for ADL7078

**Table 7. ADL7078, 24-Lead LFCSP**

ESD Model	Withstand Threshold (V)	Class
HBM	$\pm 500$	1B

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**PIN CONFIGURATION AND FUNCTION DESCRIPTIONS**

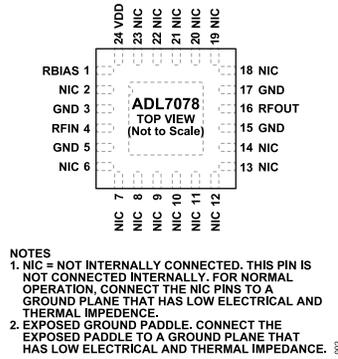


Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDD to set the $I_{DQ}$ . See Figure 3 for the interface schematic.
2, 6 to 14, 18 to 23	NIC	Not Internally Connected. This pin is not connected internally. For normal operation, connect the NIC pins to a ground plane that has low electrical and thermal impedance.
3, 5, 15, 17	GND	Ground. Connect the GND pins to a ground plane that has low electrical and thermal impedance. See Figure 4 for the interface schematic.
4	RFIN	RF Input. The RFIN pin has a DC path to ground followed by an AC-coupling capacitor in the RF signal path and matched to 50 $\Omega$ . If the DC bias level of the input signal is not equal to 0 V, externally AC-couple the RFIN pin. See Figure 5 for the interface schematic.
16	RFOUT	RF Output. The RFOUT pin has a resistive path to ground and an AC-coupling capacitor in the RF signal path and matched to 50 $\Omega$ . If the DC bias level of the next stage is not equal to 0 V, externally AC-couple the RFOUT pin. See Figure 5 for the interface schematic.
24	VDD EXPOSED PADDLE	Drain Bias. Connect the VDD pin to the supply voltage. See Figure 6 for the interface schematic. Exposed Ground Paddle. Connect the exposed paddle to a ground plane that has low electrical and thermal impedance.

**INTERFACE SCHEMATICS**

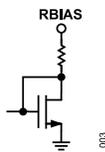


Figure 3. RBIAS Interface Schematic



Figure 4. GND Interface Schematic

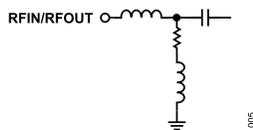


Figure 5. RFIN/RFOUT Interface Schematic

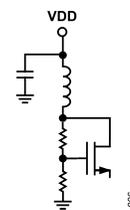


Figure 6. VDD Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

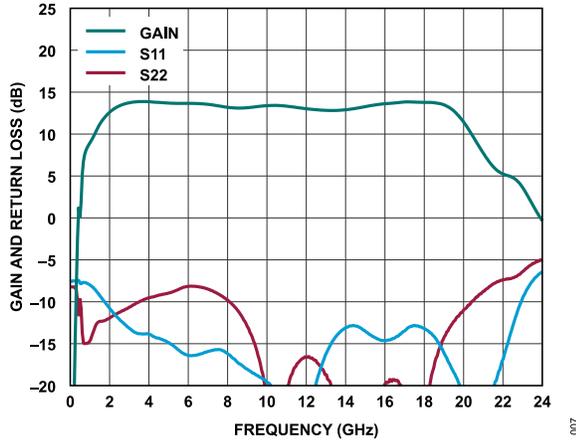


Figure 7. Broadband Gain and Return Loss vs. Frequency,  $V_{DD} = 5\text{ V}$ ,  $I_{DQ} = 175\text{ mA}$ ,  $R_{BIAS} = 698\ \Omega$

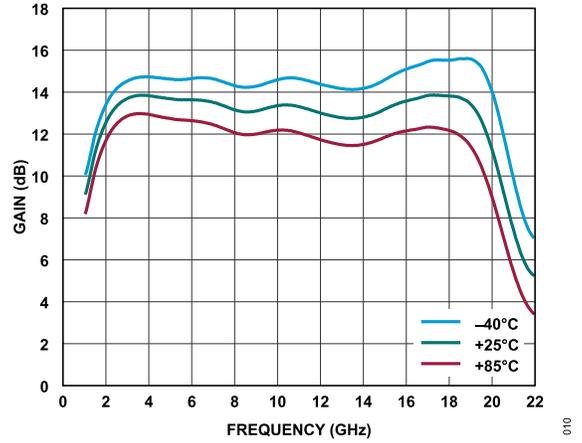


Figure 10. Gain vs. Frequency for Various Temperatures,  $V_{DD} = 5\text{ V}$ ,  $I_{DQ} = 175\text{ mA}$ ,  $R_{BIAS} = 698\ \Omega$

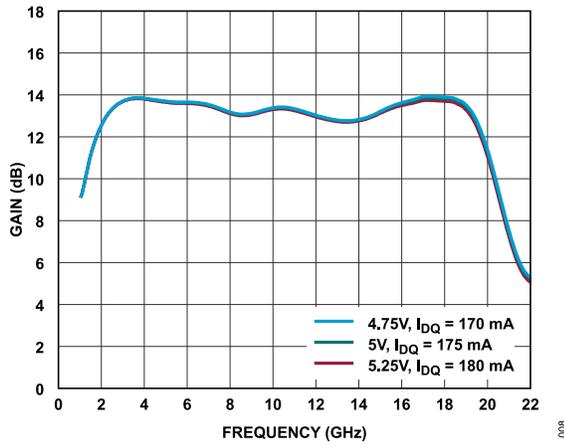


Figure 8. Gain vs. Frequency for Various Supply Voltages and  $I_{DQ}$  Values,  $R_{BIAS} = 698\ \Omega$

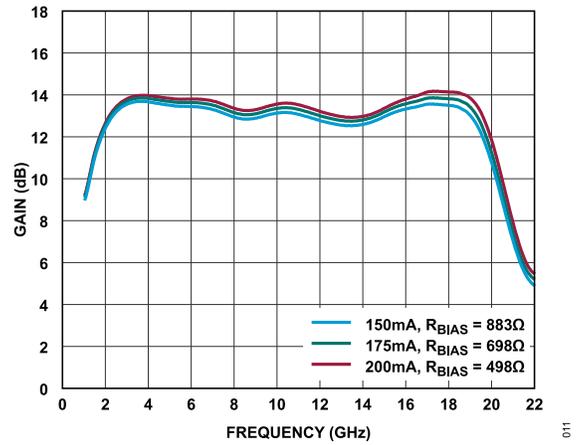


Figure 11. Gain vs. Frequency for Various  $I_{DQ}$  and  $R_{BIAS}$  Values,  $V_{DD} = 5\text{ V}$

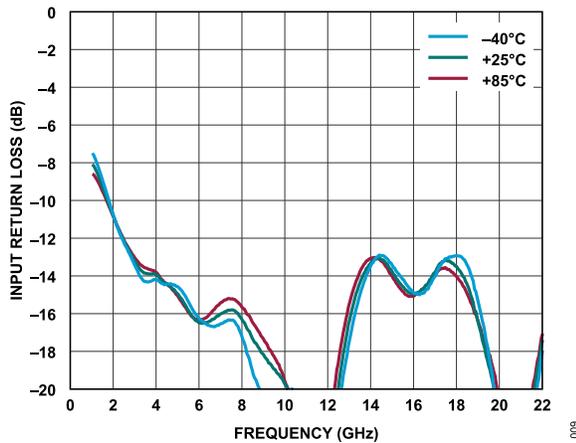


Figure 9. Input Return Loss vs. Frequency for Various Temperatures,  $V_{DD} = 5\text{ V}$ ,  $I_{DQ} = 175\text{ mA}$ ,  $R_{BIAS} = 698\ \Omega$

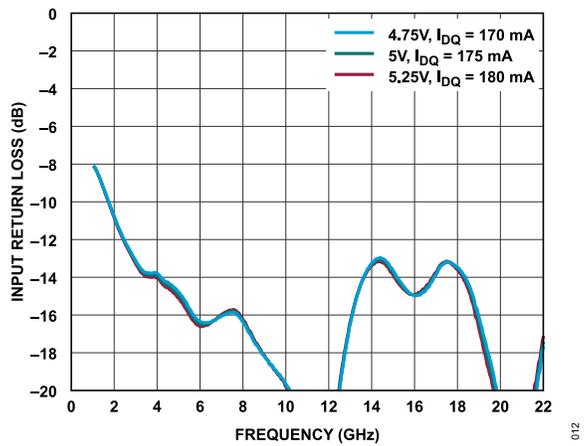


Figure 12. Input Return Loss vs. Frequency for Various  $V_{DD}$  and  $I_{DQ}$  Values,  $R_{BIAS} = 698\ \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

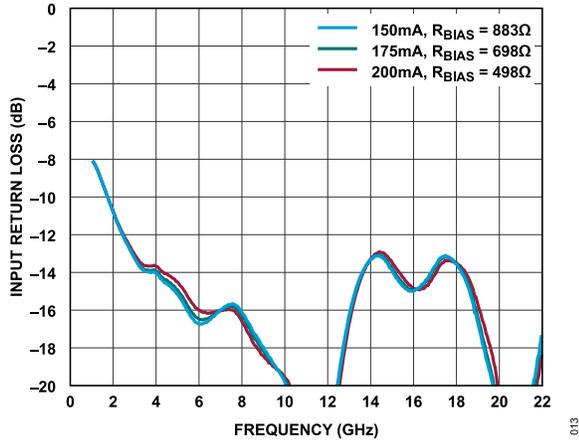


Figure 13. Input Return Loss vs. Frequency for Various  $I_{DQ}$  and  $R_{BIAS}$  Values,  $V_{DD} = 5\text{ V}$

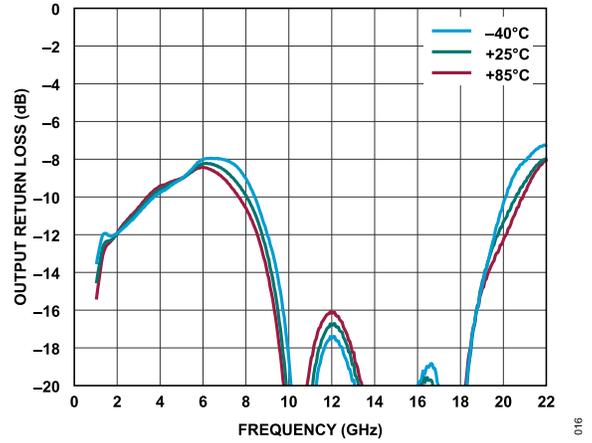


Figure 16. Output Return Loss vs. Frequency for Various Temperatures,  $V_{DD} = 5\text{ V}$ ,  $I_{DQ} = 175\text{ mA}$ ,  $R_{BIAS} = 698\ \Omega$

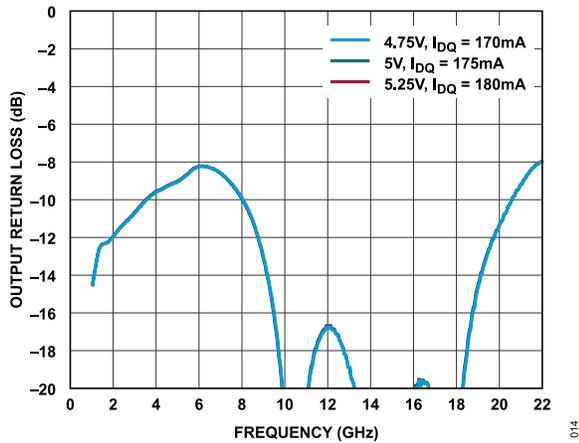


Figure 14. Output Return Loss vs. Frequency for Various  $V_{DD}$  and  $I_{DQ}$  Values,  $R_{BIAS} = 698\ \Omega$

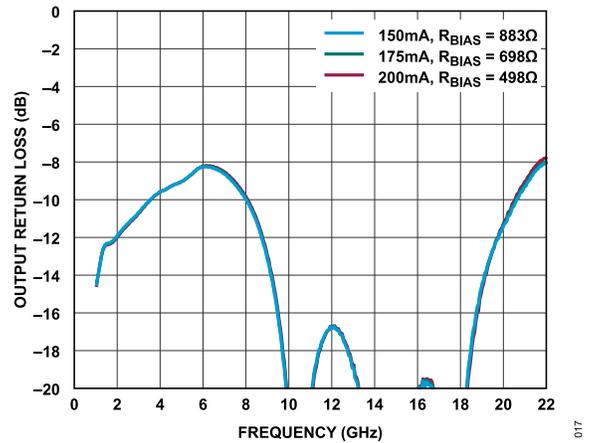


Figure 17. Output Return Loss vs. Frequency for Various  $I_{DQ}$  and  $R_{BIAS}$  Values,  $V_{DD} = 5\text{ V}$

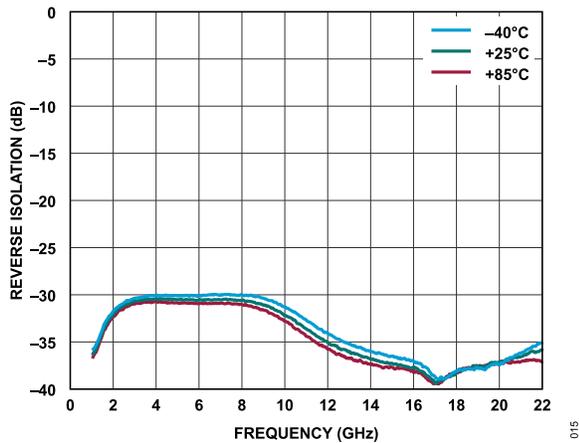


Figure 15. Reverse Isolation vs. Frequency for Various Temperatures,  $V_{DD} = 5\text{ V}$ ,  $I_{DQ} = 175\text{ mA}$ ,  $R_{BIAS} = 698\ \Omega$

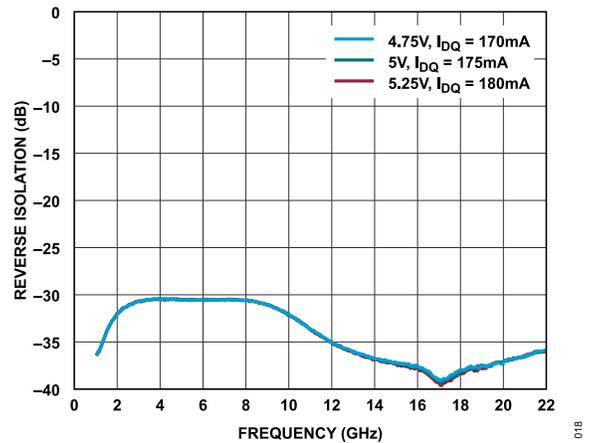


Figure 18. Reverse Isolation vs. Frequency for Various  $V_{DD}$  and  $I_{DQ}$  Values,  $R_{BIAS} = 698\ \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

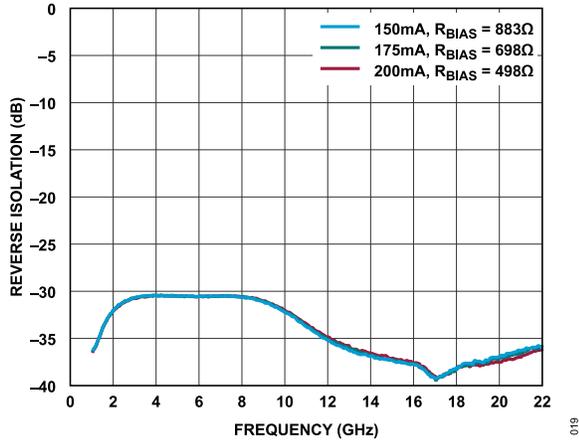


Figure 19. Reverse Isolation vs. Frequency for Various  $I_{DQ}$  and  $R_{BIAS}$  Values,  $V_{DD} = 5\text{ V}$

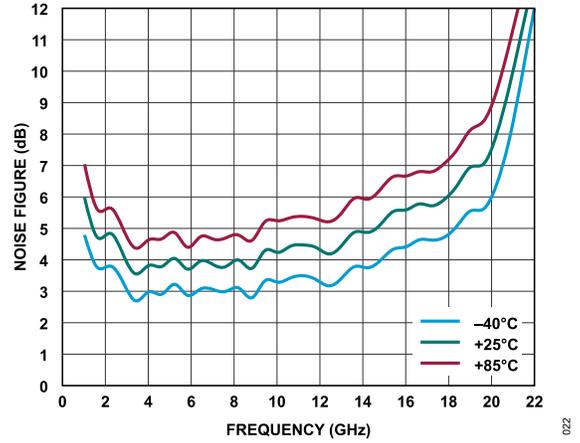


Figure 22. Noise Figure vs. Frequency for Various Temperatures,  $V_{DD} = 5\text{ V}$ ,  $I_{DQ} = 175\text{ mA}$ ,  $R_{BIAS} = 698\ \Omega$

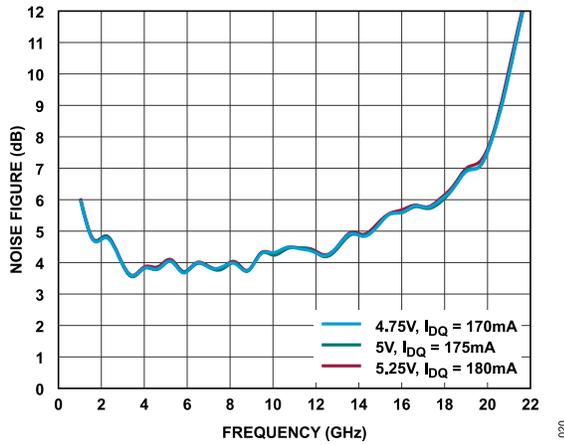


Figure 20. Noise Figure vs. Frequency for Various  $V_{DD}$  and  $I_{DQ}$  Values,  $R_{BIAS} = 698\ \Omega$

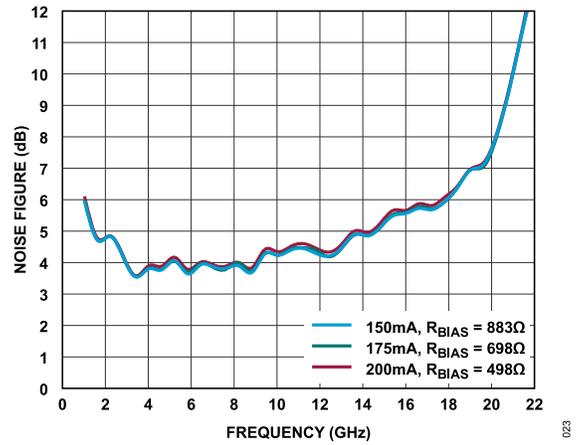


Figure 23. Noise Figure vs. Frequency for Various  $I_{DQ}$  and  $R_{BIAS}$  Values,  $V_{DD} = 5\text{ V}$

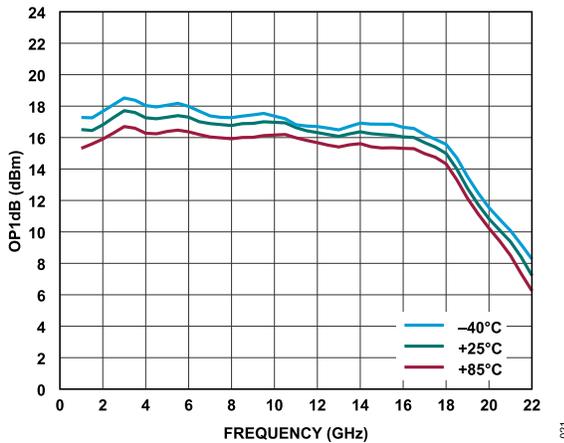


Figure 21. OP1dB vs. Frequency for Various Temperatures,  $V_{DD} = 5\text{ V}$ ,  $I_{DQ} = 175\text{ mA}$ ,  $R_{BIAS} = 698\ \Omega$

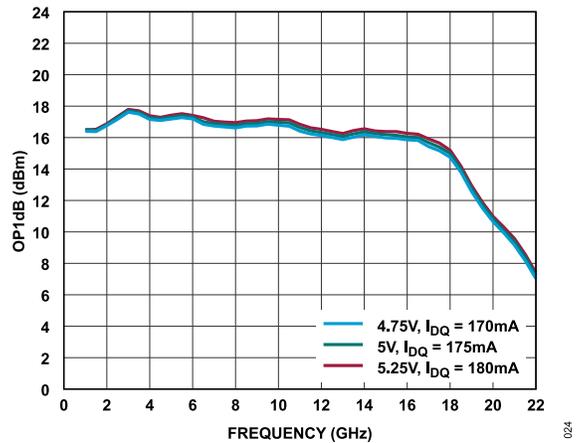


Figure 24. OP1dB vs. Frequency for Various  $V_{DD}$  and  $I_{DQ}$  Values,  $R_{BIAS} = 698\ \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

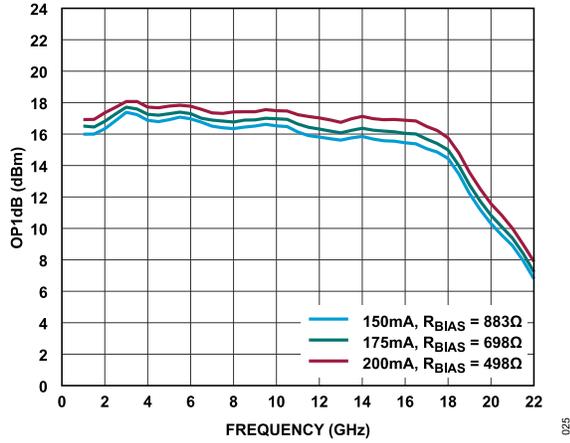


Figure 25. OP1dB vs. Frequency for Various  $I_{DQ}$  and  $R_{BIAS}$  Values,  $V_{DD} = 5\text{ V}$

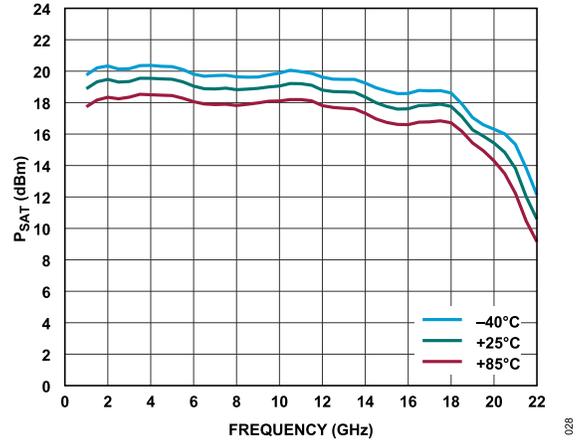


Figure 28.  $P_{SAT}$  vs. Frequency for Various Temperatures,  $V_{DD} = 5\text{ V}$ ,  $I_{DQ} = 175\text{ mA}$ ,  $R_{BIAS} = 698\ \Omega$

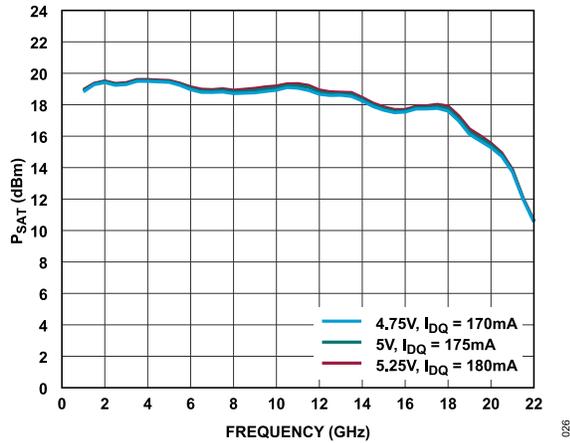


Figure 26.  $P_{SAT}$  vs. Frequency for Various  $V_{DD}$  and  $I_{DQ}$  Values,  $R_{BIAS} = 698\ \Omega$

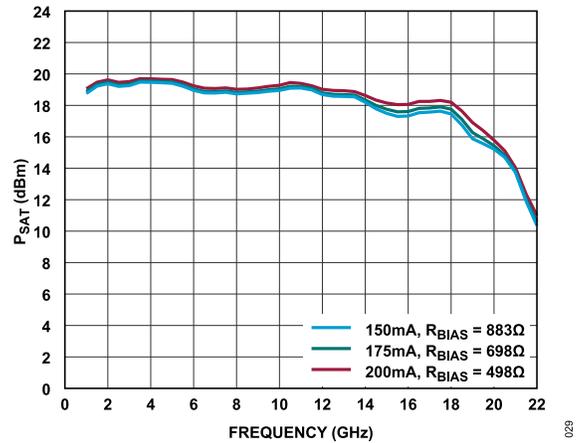


Figure 29.  $P_{SAT}$  vs. Frequency for Various  $I_{DQ}$  and  $R_{BIAS}$  Values,  $V_{DD} = 5\text{ V}$

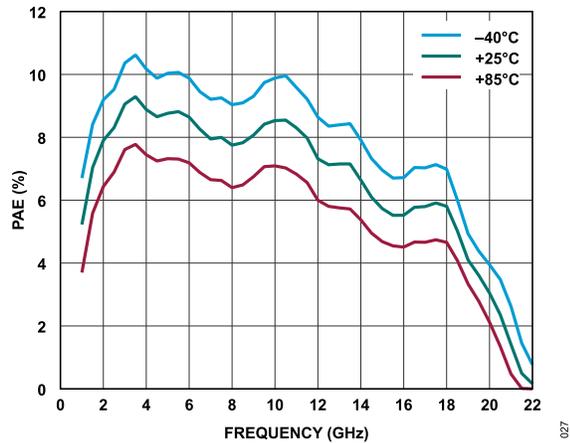


Figure 27. PAE Measured at  $P_{SAT}$  vs. Frequency for Various Temperatures,  $V_{DD} = 5\text{ V}$ ,  $I_{DQ} = 175\text{ mA}$ ,  $R_{BIAS} = 698\ \Omega$

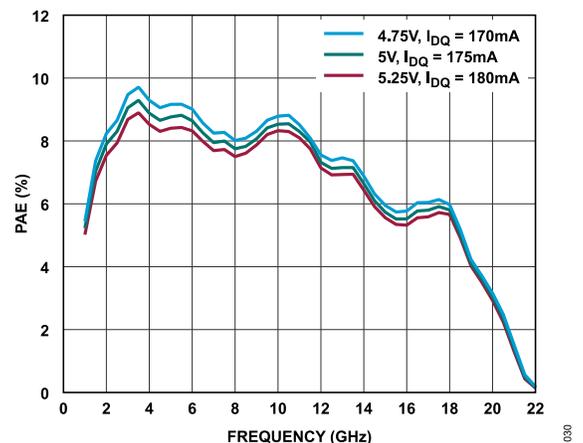


Figure 30. PAE Measured at  $P_{SAT}$  vs. Frequency for Various  $V_{DD}$  and  $I_{DQ}$  Values,  $R_{BIAS} = 698\ \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

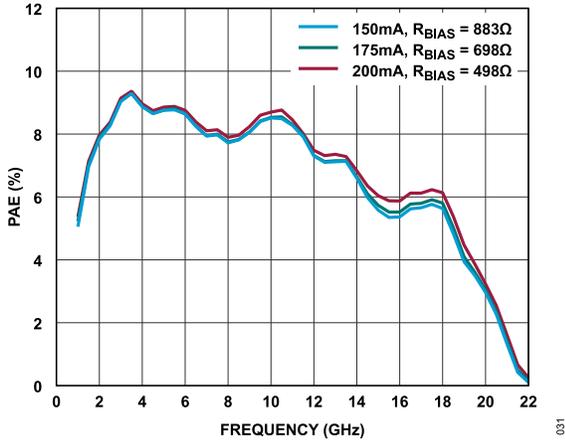


Figure 31. PAE Measured at  $P_{SAT}$  vs. Frequency for Various  $I_{DD}$  and  $R_{BIAS}$  Values,  $V_{DD} = 5 V$

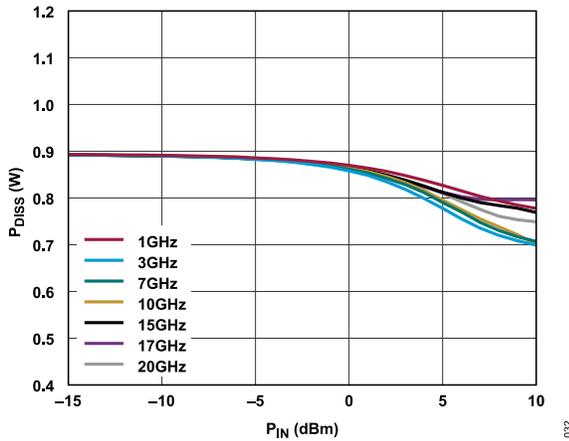


Figure 32.  $P_{DISS}$  vs.  $P_{IN}$  at Various Frequencies, Temperature =  $85^{\circ}C$ ,  $V_{DD} = 5 V$ ,  $I_{DD} = 175 mA$ ,  $R_{BIAS} = 698 \Omega$

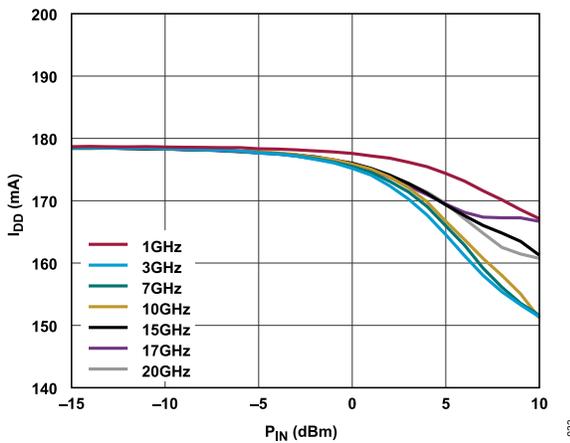


Figure 33.  $I_{DD}$  vs.  $P_{IN}$  for Various Frequencies, Temperature =  $85^{\circ}C$ ,  $V_{DD} = 5 V$ ,  $R_{BIAS} = 698 \Omega$

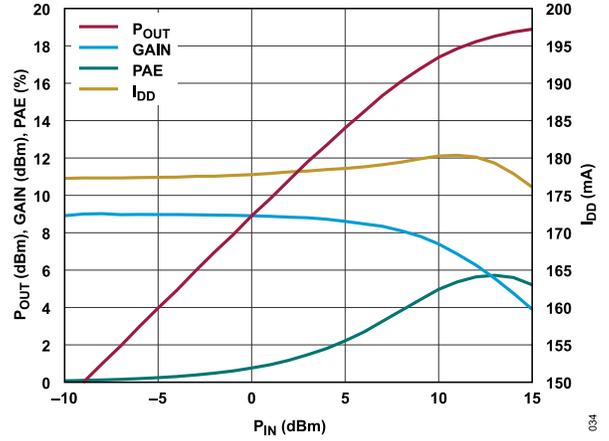


Figure 34.  $P_{OUT}$ , Gain, PAE, and  $I_{DD}$  vs.  $P_{IN}$  at 1 GHz,  $V_{DD} = 5 V$ ,  $R_{BIAS} = 698 \Omega$

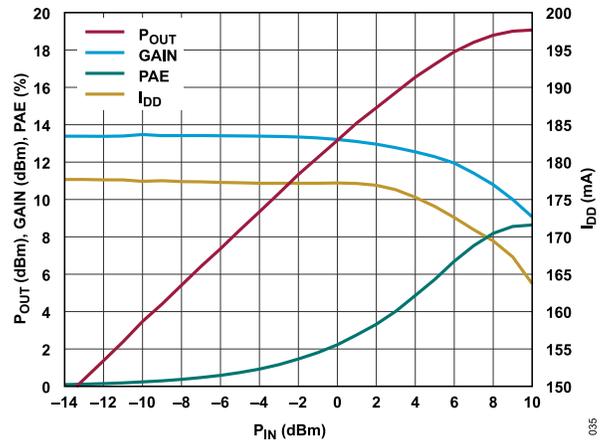


Figure 35.  $P_{OUT}$ , Gain, PAE, and Supply Current ( $I_{DD}$ ) vs.  $P_{IN}$  at 10 GHz,  $V_{DD} = 5 V$ ,  $R_{BIAS} = 698 \Omega$

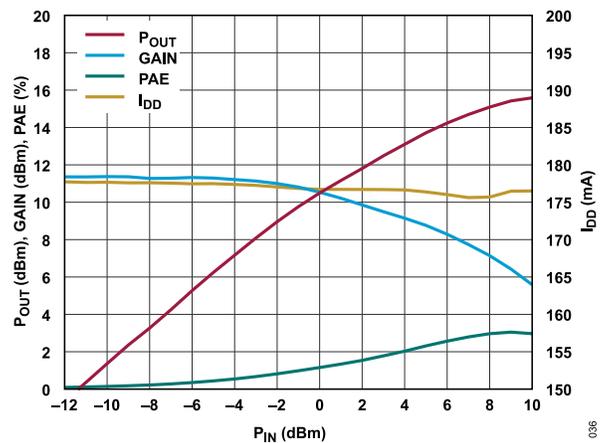


Figure 36.  $P_{OUT}$ , Gain, PAE, and  $I_{DD}$  vs.  $P_{IN}$  at 20 GHz,  $V_{DD} = 5 V$ ,  $R_{BIAS} = 698 \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

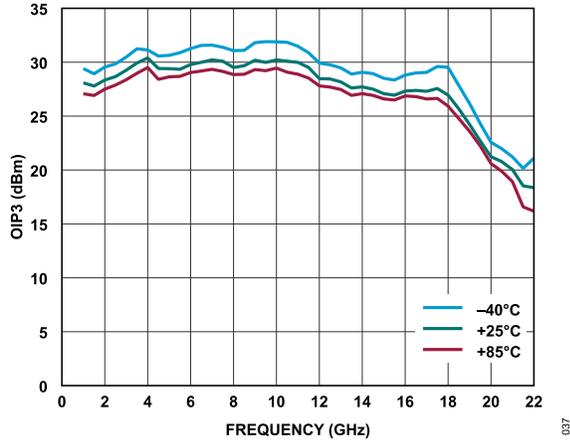


Figure 37. OIP3 vs. Frequency for Various Temperatures,  $P_{OUT}$  per Tone = 0 dBm,  $V_{DD}$  = 5 V,  $I_{DQ}$  = 175 mA,  $R_{BIAS}$  = 698  $\Omega$

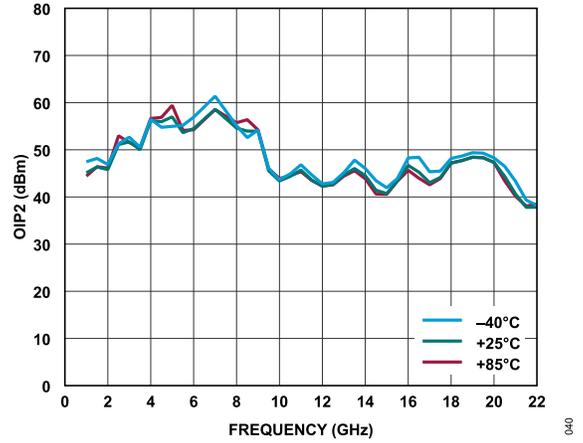


Figure 40. OIP2 vs. Frequency for Various Temperatures,  $P_{OUT}$  per Tone = 0 dBm,  $V_{DD}$  = 5 V,  $I_{DQ}$  = 175 mA,  $R_{BIAS}$  = 698  $\Omega$

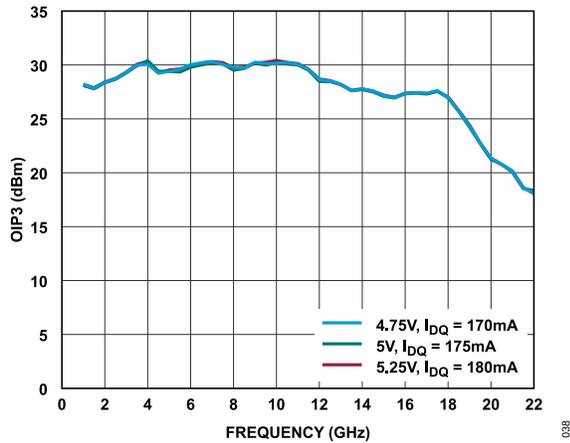


Figure 38. OIP3 vs. Frequency for Various  $V_{DD}$  and  $I_{DQ}$  Values,  $P_{OUT}$  per Tone = 0 dBm,  $R_{BIAS}$  = 698  $\Omega$

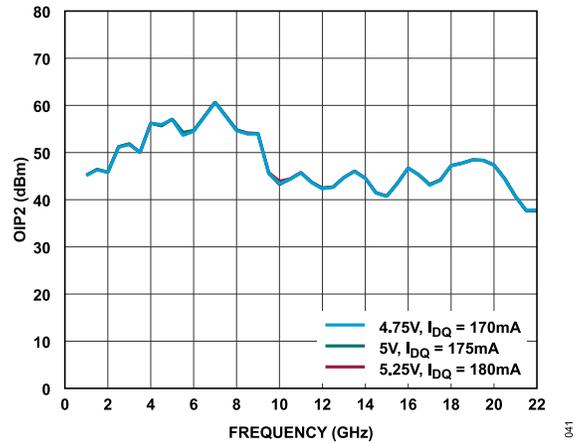


Figure 41. OIP2 vs. Frequency for Various  $V_{DD}$  and  $I_{DQ}$  Values,  $P_{OUT}$  per Tone = 0 dBm,  $R_{BIAS}$  = 698  $\Omega$

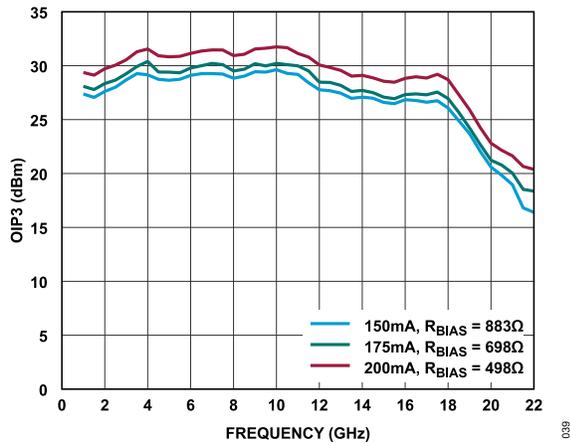


Figure 39. OIP3 vs. Frequency for Various  $I_{DQ}$  and  $R_{BIAS}$  Values,  $P_{OUT}$  per Tone = 0 dBm,  $V_{DD}$  = 5 V

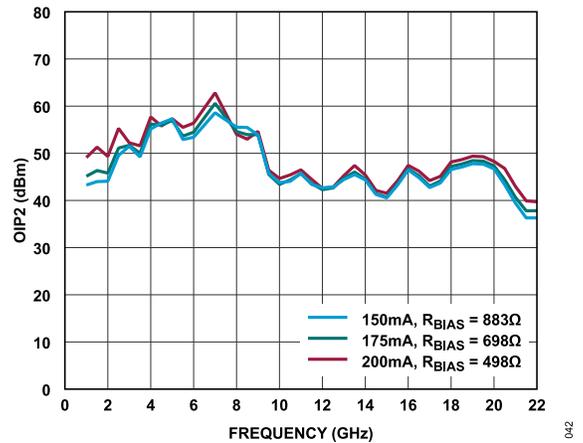


Figure 42. OIP2 vs. Frequency for Various  $I_{DQ}$  and  $R_{BIAS}$  Values,  $P_{OUT}$  per Tone = 0 dBm,  $V_{DD}$  = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

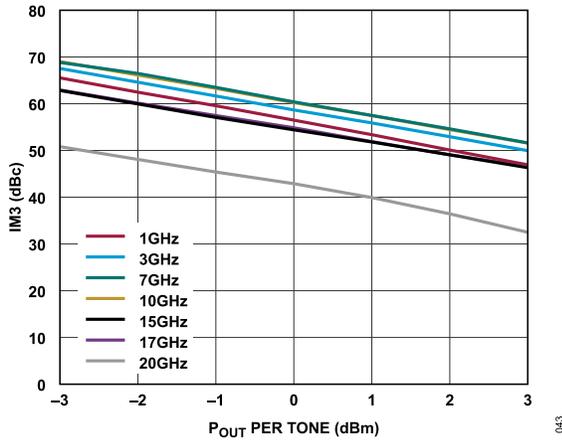


Figure 43. Third-Order Intermodulation (IM3) vs.  $P_{OUT}$  per Tone for Various Frequencies,  $V_{DD} = 4.75\text{ V}$ ,  $I_{DQ} = 170\text{ mA}$ ,  $R_{BIAS} = 698\ \Omega$

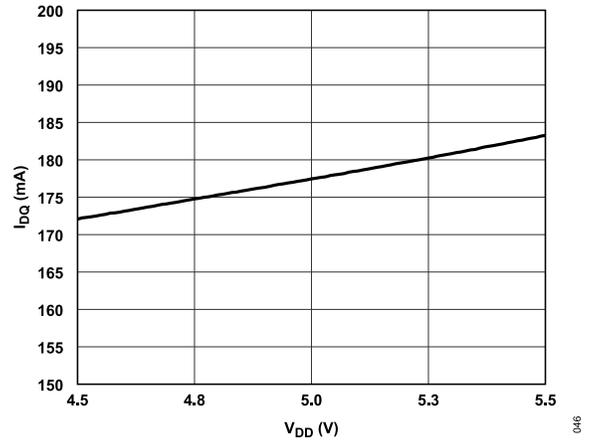


Figure 46.  $I_{DQ}$  vs.  $V_{DD}$ ,  $R_{BIAS} = 698\ \Omega$

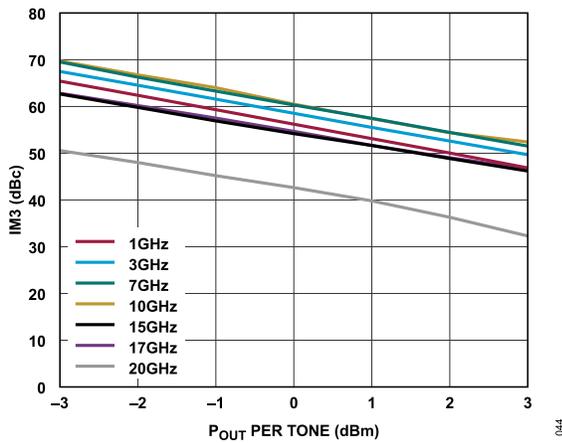


Figure 44. IM3 vs.  $P_{OUT}$  per Tone for Various Frequencies,  $V_{DD} = 5\text{ V}$ ,  $I_{DQ} = 175\text{ mA}$ ,  $R_{BIAS} = 698\ \Omega$

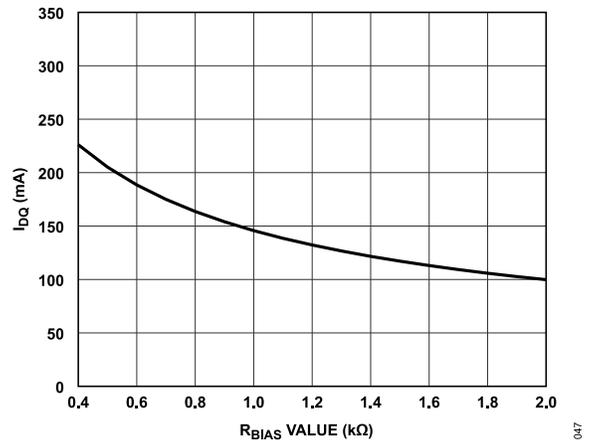


Figure 47.  $I_{DQ}$  vs.  $R_{BIAS}$  Value

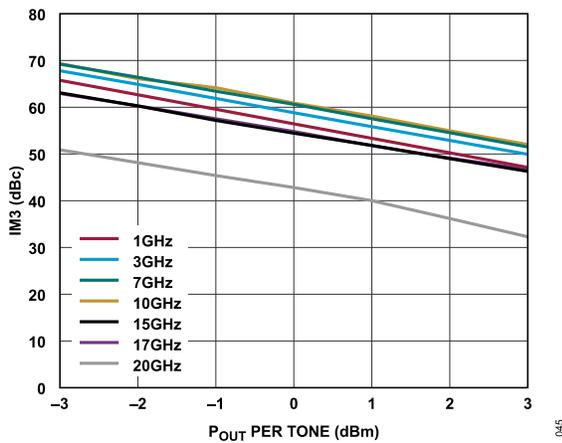


Figure 45. IM3 vs.  $P_{OUT}$  per Tone for Various Frequencies,  $V_{DD} = 5.25\text{ V}$ ,  $I_{DQ} = 180\text{ mA}$ ,  $R_{BIAS} = 698\ \Omega$

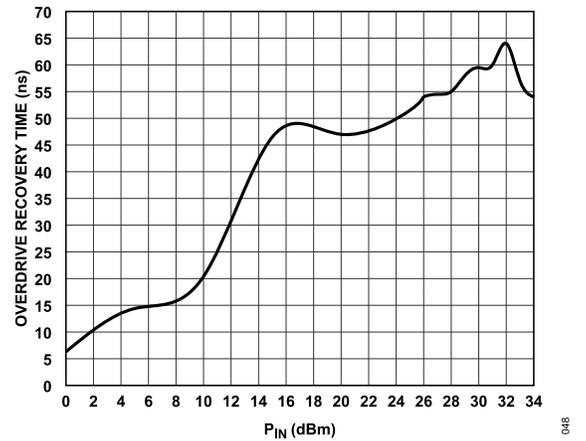


Figure 48. Overdrive Recovery Time vs.  $P_{IN}$  at 9.6 GHz, Recovery to Within 90% of Small Signal Gain Value (Blocking Signal at 7.5 GHz),  $V_{DD} = 5\text{ V}$ ,  $R_{BIAS} = 698\ \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

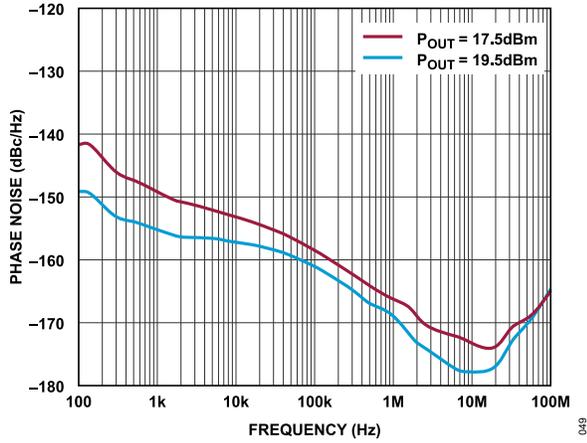


Figure 49. Phase Noise vs. Frequency at 5 GHz for Various P<sub>OUT</sub> Values

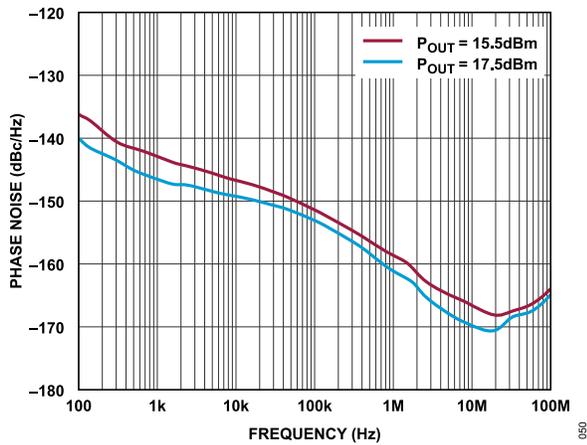


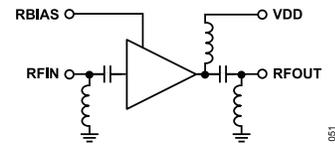
Figure 50. Phase Noise vs. Frequency at 15 GHz for Various P<sub>OUT</sub> Values

## THEORY OF OPERATION

The ADL7078 is a low-noise, wideband amplifier with integrated AC-coupling capacitors and a bias inductor. A simplified block diagram is shown in [Figure 51](#).

The ADL7078 RFIN and RFOUT pins are AC-coupled and matched to 50  $\Omega$ . However, if these pins are connecting to devices with bias levels that are not equal to 0 V, externally AC-couple the RFIN and RFOUT pins.

To adjust the drain bias current, connect an external resistor between the RBIAS and VDD pins.



**Figure 51. Simplified Schematic**

## APPLICATIONS INFORMATION

The basic connections for operating the ADL7078 over the specified frequency range are shown in Figure 52. No external biasing inductor is required, allowing the 5 V supply to be connected to the VDD pin. Power supply decoupling capacitors of 0.01  $\mu\text{F}$  and 100 pF are recommended. No AC coupling capacitors are required on RFIN or on RFOUT as long as these pins are connected to DC bias levels of 0 V.

To set the  $I_{DQ}$ , connect a resistor between the RBIAS and VDD pins. A default value of 698  $\Omega$  is recommended, which results in a nominal  $I_{DQ}$  of 175 mA, supplying 5 V to VDD pin. Table 9 details the resulting  $I_{DQ}$  for various  $R_{BIAS}$  values where the resistor is tied to 5 V.

The circuit shown in Figure 52 represents the configuration used to characterize and qualify the ADL7078.

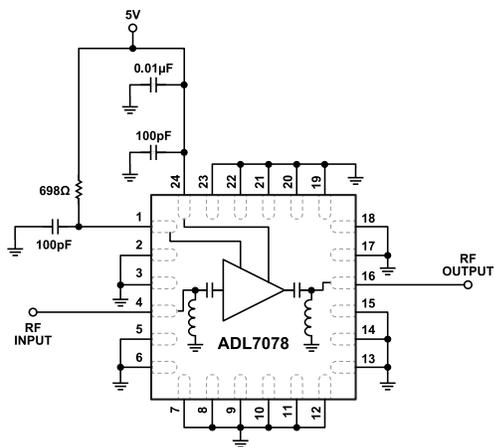


Figure 52. Typical Application Circuit

To safely operate the ADL7078, apply RF power after the supply voltage is connected to VDD and RBIAS and remove the RF power before the supply voltage is removed from VDD and RBIAS.

Table 9. Recommended  $R_{BIAS}$  Values for  $V_{DD} = 5\text{ V}$

$R_{BIAS}$ ( $\Omega$ )	$I_{DQ}$ (mA)	$I_{DQ\_AMP}$ (mA)	$I_{RBIAS}$ (mA)
498	200	194.5	5.5
698	175	170.5	4.5
883	150	146	3.8

## RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 53 shows the recommended power management circuit for the ADL7078. The LT8607 step-down regulator is used to step down a 12 V rail to 6.62 V, which is then applied to the LT3042 low dropout (LDO) linear regulator to generate a low noise 5 V output. While the circuit shown in Figure 53 has an input voltage ( $V_{IN}$ ) of 12 V, the input range to the LT8607 can be as high as 42 V.

The 6.62 V regulator output of the LT8607 is set by the R2 and R3 resistors according to the following equation:

$$R2 = R3((V_{OUT}/0.778 \text{ V}) - 1), \text{ where } V_{OUT} \text{ is the output voltage.}$$

The switching frequency ( $f_{SW}$ ) is set to 2 MHz by the 18.2 k $\Omega$  resistor on the RT pin of the LT8697. The LT8607 data sheet

provides a table of resistor values that can be used to select other  $f_{SW}$  values ranging from 0.2 MHz to 2.200 MHz.

$$V_{OUT} = 100 \mu\text{A} \times R4$$

The PGFB resistors of the LT3042 are chosen to trigger the power-good (PG) signal when the output is just under 95% of the target voltage of 5 V. The output of the LT3042 has 1% initial tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature and adding resistors results in a bit more (5%), therefore, putting 5% between the output and the PGFB resistors works well. In addition, the PG open collector is pulled up to the 5 V output to give a convenient 0 V to 5 V voltage range.

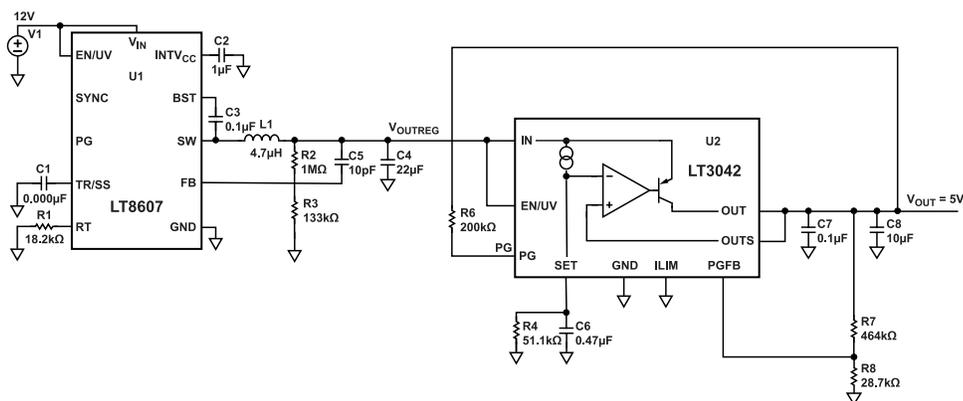


Figure 53. Recommended Power Management Circuit

USING THE RBIAS PIN TO ENABLE AND DISABLE THE ADL7078

By attaching a SPDT switch to the RBIAS resistor, an enable and disable circuit can be implemented as shown in Figure 54. The ADG719 CMOS switch is used to connect the RBIAS resistor either to a supply or ground. When the RBIAS resistor is connected to ground, the overall current consumption reduces to 3.61 mA with no RF signal present and 3.75 mA when the RF input level is 0 dBm. Figure 55 shows a plot of the turn on and the turn off response time of the RF output envelope when the IN pin of the ADG719 is pulsed.

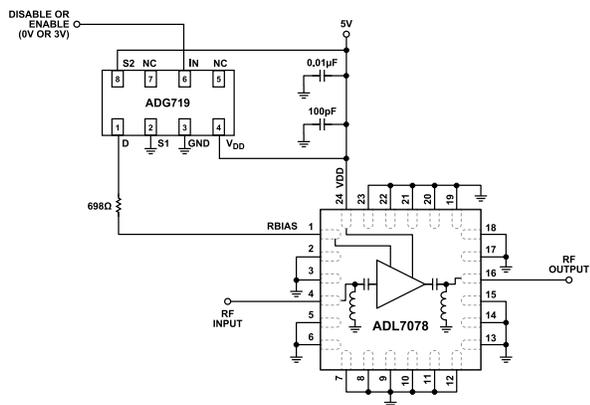


Figure 54. Fast Enable or Disable Using a 0 V or 3 V Pulse on the RBIAS Pin

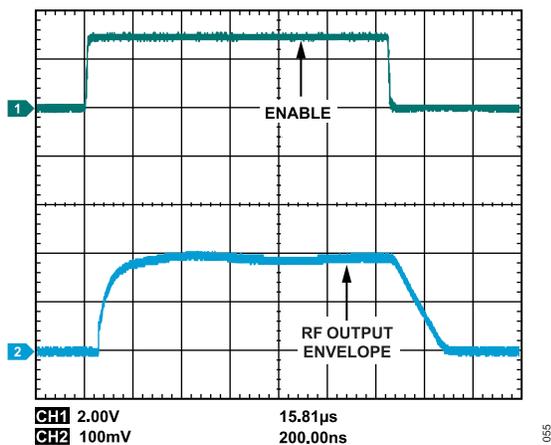
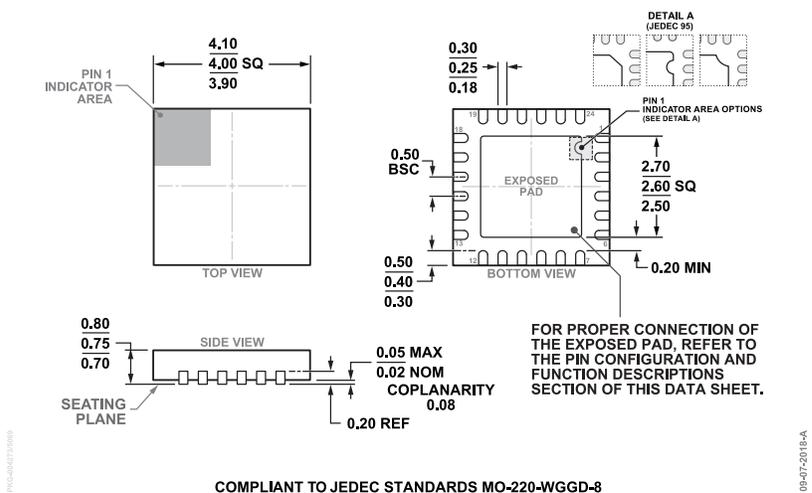


Figure 55. Turn-On and Turn-Off Response Time of the RF Output Envelope when the IN Pin of the ADG719 Is Pulsed

OUTLINE DIMENSIONS



**Figure 56. 24-Lead Lead Frame Chip Scale Package [LFCSP]  
4 mm x 4 mm Body and 0.75 mm Package Height  
(CP-24-15)  
Dimensions shown in millimeters**

Updated: October 12, 2023

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Packing Quantity	Package Option
ADL7078ACPZN	-40°C to +85°C	24-Lead LFCSP (4 mm x 4 mm with EP)		CP-24-15
ADL7078ACPZN-R7	-40°C to +85°C	24-Lead LFCSP (4 mm x 4 mm with EP)	Reel, 1500	CP-24-15

<sup>1</sup> Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 10. Evaluation Boards

Model <sup>1</sup>	Description
ADL7078-EVALZ	Evaluation Board

<sup>1</sup> Z = RoHS-Compliant Part.