Data Sheet

ADPA9007-2

DC to 28 GHz, GaAs, pHEMT, 2 W Power Amplifier

FEATURES

- Wideband, internally matched, RF power amplifier
- DC-coupled input and output
- Integrated RF power detector
- Integrated temperature sensor
- Gain: 13 dB typical at 8 GHz to 16 GHz
- OP1dB: 32.5 dBm typical at 8 GHz to 16 GHz
- P_{SAT}: 33.5 dBm typical at 8 GHz to 16 GHz
- OIP3: 43.5 dBm typical at 8 GHz to 16 GHz

APPLICATIONS

- Electronic warfare
- Radar
- Test and measurement equipment

GENERAL DESCRIPTION

The ADPA9007-2CHIP is a 2 W, RF power amplifier that operates from DC to 28 GHz. The RF input and output are internally matched and DC-coupled. The ADPA9007-2CHIP includes an integrated temperature-compensated RF power detector and an integrated temperature sensor.

The ADPA9007-2CHIP amplifier provides a gain of 13 dB, an output power for 1 dB compression (OP1dB) of 32.5 dBm, and an output third-order intercept (OIP3) of 43.5 dBm from 8 GHz to 16 GHz. The amplifier operates from a typical supply voltage (V_{DD}) of 15 V and has a 500 mA typical quiescent drain current (I_{DQ}), which is adjustable.

The ADPA9007-2CHIP is fabricated on a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT) process and is specified for operation from −55°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

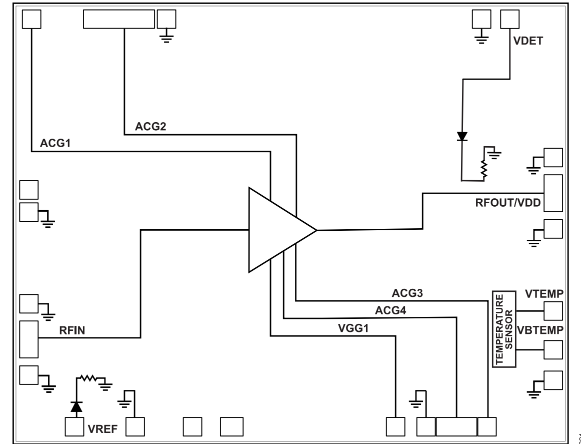

Figure 1. Functional Block Diagram

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

4/2024—Revision 0: Initial Version

SPECIFICATIONS

0.05 GHz TO 8 GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD} = 15 V, and I_{DQ} = 500 mA, unless otherwise noted. Adjust the gate voltage (V_{GG1}) from −1.5 V to 0 V to achieve I_{DQ} = 500 mA typical.

Table 1. 0.05 GHz to 8 GHz Frequency Range

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		0.05		8	GHz
GAIN		11	13		dB
Flatness			±0.5		dB
Variation over Temperature			0.015		dB/°C
NOISE FIGURE			8		dB
RETURN LOSS					
Input			13		dB
Output			14		dB
OUTPUT					
OP1dB		31	33		dBm
Saturated Output Power (P_{SAT})			35		dBm
OIP3	Output power (P_{OUT}) per tone = 16 dBm with 1 MHz tone spacing		43		dBm
OIP2	P_{OUT} per tone = 16 dBm with 1 MHz tone spacing		48		dBm
SUPPLY					
I_{DQ}	Adjust V_{GG1} to achieve I_{DQ} = 500 mA typical		500		mA
V_{DD}		10		15	V

8 GHz TO 16 GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD} = 15 V, and I_{DQ} = 500 mA, unless otherwise noted. Adjust V_{GG1} from −1.5 V to 0 V to achieve I_{DQ} = 500 mA typical.

Table 2. 8 GHz to 16 GHz Frequency Range

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		8		16	GHz
GAIN		11	13		dB
Flatness			±0.2		dB
Variation over Temperature			0.006		dB/°C
NOISE FIGURE			3.5		dB
RETURN LOSS					
Input			15		dB
Output			16		dB
OUTPUT					
OP1dB		30.5	32.5		dBm
P_{SAT}			33.5		dBm
OIP3	P_{OUT} per tone = 16 dBm with 1 MHz tone spacing		43.5		dBm
OIP2	P_{OUT} per tone = 16 dBm with 1 MHz tone spacing		42.5		dBm
SUPPLY					
I_{DQ}	Adjust V_{GG1} to achieve I_{DQ} = 500 mA typical		500		mA
V_{DD}		10		15	V

SPECIFICATIONS

16 GHz TO 20 GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD} = 15 V, and I_{DQ} = 500 mA, unless otherwise noted. Adjust V_{GG1} from −1.5 V to 0 V to achieve I_{DQ} = 500 mA typical.

Table 3. 16 GHz to 20 GHz Frequency Range

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		16		20	GHz
GAIN		11	13		dB
Flatness			±0.15		dB
Variation over Temperature			0.007		dB/°C
NOISE FIGURE			3.5		dB
RETURN LOSS					
Input			16		dB
Output			16		dB
OUTPUT					
OP1dB		29	31		dBm
P_{SAT}			32.5		dBm
OIP3	P_{OUT} per tone = 16 dBm with 1 MHz tone spacing		41		dBm
OIP2	P_{OUT} per tone = 16 dBm with 1 MHz tone spacing		41		dBm
SUPPLY					
I_{DQ}	Adjust V_{GG1} to achieve I_{DQ} = 500 mA typical		500		mA
V_{DD}		10		15	V

20 GHz TO 24 GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD} = 15 V, and I_{DQ} = 500 mA, unless otherwise noted. Adjust the V_{GG1} from −1.5 V to 0 V to achieve I_{DQ} = 500 mA typical

Table 4. 20 GHz to 24 GHz Frequency Range

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		20		24	GHz
GAIN		11	13		dB
Flatness			±0.28		dB
Variation over Temperature			0.01		dB/°C
NOISE FIGURE			4		dB
RETURN LOSS					
Input			17		dB
Output			18		dB
OUTPUT					
OP1dB		27	29		dBm
P_{SAT}			31		dBm
OIP3	P_{OUT} per tone = 16 dBm with 1 MHz spacing		42		dBm
OIP2	P_{OUT} per tone = 16 dBm with 1 MHz spacing		45		dBm
SUPPLY					
I_{DQ}	Adjust V_{GG1} to achieve I_{DQ} = 500 mA typical		500		mA
V_{DD}		10		15	V

SPECIFICATIONS

24 GHz TO 28 GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD} = 15 V, and I_{DQ} = 500 mA, unless otherwise noted. Adjust the V_{GG1} from −1.5 V to 0 V to achieve I_{DQ} = 500 mA typical.

Table 5. 24 GHz to 28 GHz Frequency Range

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		24		28	GHz
GAIN		10.5	12.5		dB
Flatness			±0.3		dB
Variation over Temperature			0.011		
NOISE FIGURE			4.5		dB
RETURN LOSS					
Input			17		dB
Output			17		dB
OUTPUT					
OP1dB		26	28		dBm
P_{SAT}			30		dBm
OIP3	P_{OUT} per tone = 16 dBm with 1 MHz tone spacing		40		dBm
SUPPLY					
I_{DQ}	Adjust V_{GG1} to achieve I_{DQ} = 500 mA typical		500		mA
V_{DD}		10		15	V

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	16.0 V
V_{GG1}	−2.0 V to 0 V
RF Input Power (RFIN)	29 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 143 mW/°C Above 85°C)	12.8 W
Temperature	
Maximum Channel	175°C
Quiescent Channel (T_{CASE} = 85°C, V_{DD} = 15 V), I_{DQ} = 500 mA, and Input Power (P_{IN}) = Off	137.5°C
Storage Range	−65°C to +150°C
Operating Range	−55°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Overall thermal performance is directly linked to the carrier or substrate on which the die is mounted. Careful attention is needed with each material used in the thermal path below the IC. With an epoxy layer of nominal thickness assumed under the die, θ_{JC} is the thermal resistance from the die channel to the bottom of the epoxy layer.

Table 7. Thermal Resistance

Package Type	θ_{JC} [1]	Unit
C-24-7	7.0	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel to the bottom of the epoxy layer with the ground pad beneath the die held constant at an 85°C operating temperature.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

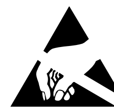
Human Body Model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADPA9007-2CHIP

Table 8. ADPA9007-2CHIP, 24-Pad CHIP

ESD Model	Withstand Threshold (V)	Class
HBM	±250	1A

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

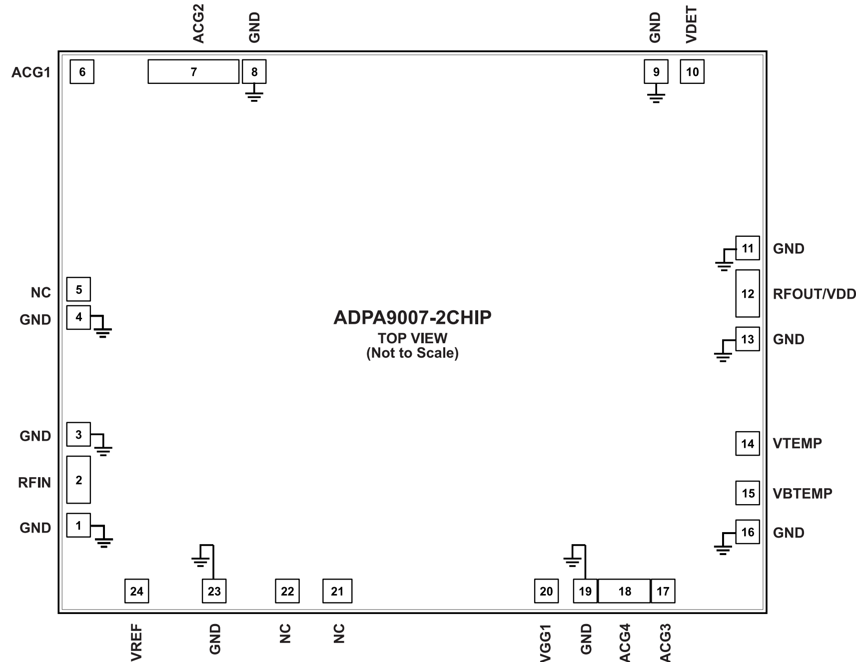


Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 8, 9, 11, 13, 16, 19, 23	GND	Ground. Do not bond these pads. See Figure 3 for the interface.
2	RFIN	RF Input of the Amplifier. The RFIN pad is DC-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
5, 21, 22	NC	No Connect. Do not connect these pads.
6	ACG1	Low Frequency Termination. Attach bypass capacitors as shown in Figure 84. See Figure 8 for the interface schematic.
7	ACG2	Low Frequency Termination. Attach bypass capacitors as shown in Figure 84. See Figure 8 for the interface schematic.
10	VDET	Detector Diode Voltage to Measure the RF Output Power. Detection by the VDET pad requires the application of a DC bias voltage through an external series resistor. Used in combination with the VREF pad, the difference detector voltage (VREF voltage (V_{REF}) − VDET voltage (V_{DET})) is a temperature compensated DC voltage proportional to the RF output power. See Figure 8 for the interface schematic.
12	RFOUT/VDD	RF Output and Drain of the Amplifier. Connect the RFOUT/VDD pad to the supply voltage (V_{DD}) network to provide the drain current (I_{DD}). See Figure 84. See the Power-Up Sequence and Power-Down Sequence for additional information. See Figure 8 for the interface schematic.
14	VTEMP	Integrated Temperature Sensor Output. See Figure 7 for the interface schematic.
15	VBTEMP	Temperature Sensor Bias. Bias pad for biasing the integrated temperature sensor. See Figure 7 for the interface schematic.
17	ACG3	Low Frequency Termination. Attach bypass capacitors as shown in Figure 84. See Figure 4 for the interface schematic.
18	ACG4	Low Frequency Termination. Attach bypass capacitors as shown in Figure 84. See Figure 4 for the interface schematic.
20	VGG1	Gate Control for the Amplifier. Attach bypass capacitors as shown in Figure 84. See the Power-Up Sequence and Power-Down Sequence for additional information. See Figure 6 for the interface schematic.
24	VREF	Reference Diode Voltage for the Temperature Compensation of the VDET RF Output Power Measurements. V_{REF} requires the application of a DC bias voltage through an external series resistor. See Figure 5 for the interface schematic.
Die Bottom	GND	Ground. Connect the die bottom to RF and dc ground. See Figure 3 for the interface schematic.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

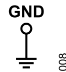


Figure 3. GND Interface Schematic

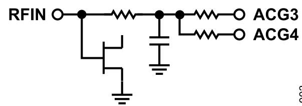


Figure 4. RFIN and ACG3 and ACG4 Interface Schematic

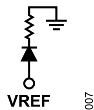


Figure 5. VREF Interface Schematic

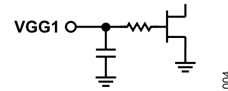


Figure 6. VGG1 Interface Schematic

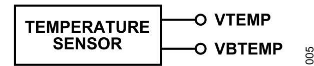


Figure 7. VTEMP and VBTEMP Interface Schematic

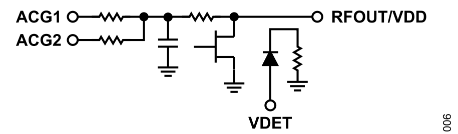


Figure 8. ACG1, ACG2, RFOUT/VDD, and VDET Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

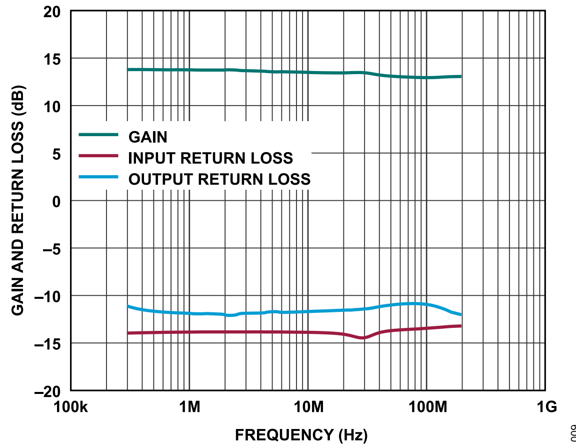


Figure 9. Gain and Return Loss vs. Frequency, 300 kHz to 200 MHz, V_{DD} = 15 V, I_{DQ} = 500 mA

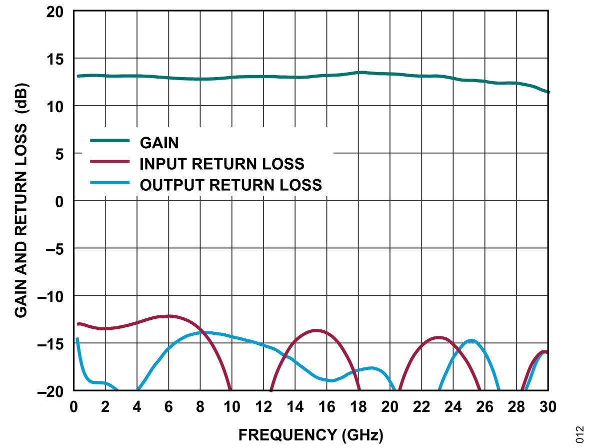


Figure 12. Gain and Return Loss vs. Frequency, 200 MHz to 30 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

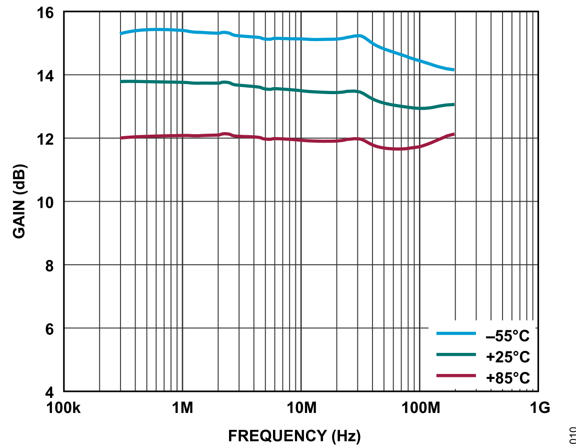


Figure 10. Gain vs. Frequency for Various Temperatures, 300 kHz to 200 MHz, V_{DD} = 15 V, I_{DQ} = 500 mA

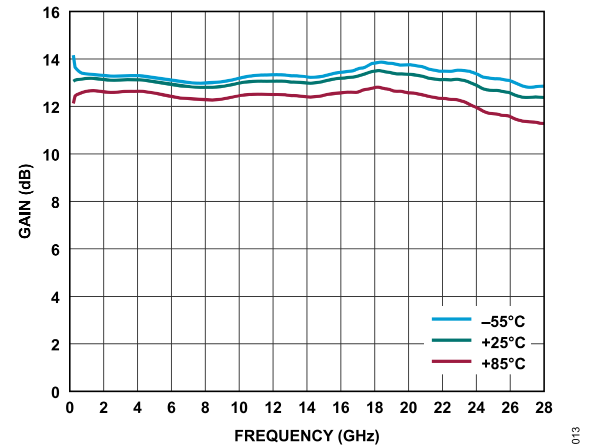


Figure 13. Gain vs. Frequency for Various Temperatures, 200 MHz to 28 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

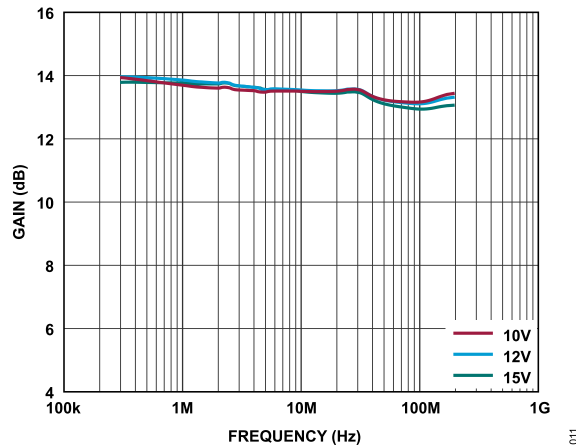


Figure 11. Gain vs. Frequency for Various V_{DD} Values, 300 kHz to 200 MHz, I_{DQ} = 500 mA

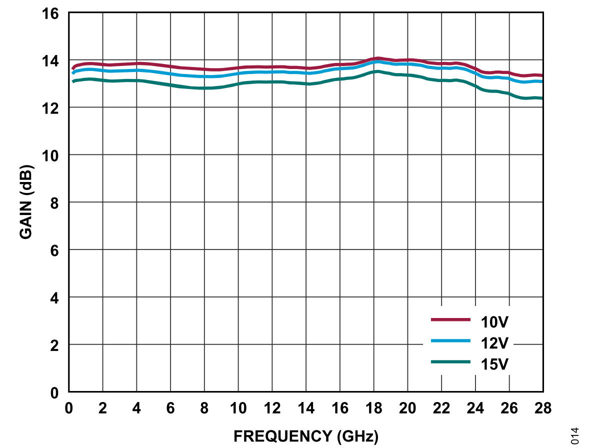


Figure 14. Gain vs. Frequency for Various V_{DD} Values, 200 MHz to 28 GHz, I_{DQ} = 500 mA

TYPICAL PERFORMANCE CHARACTERISTICS

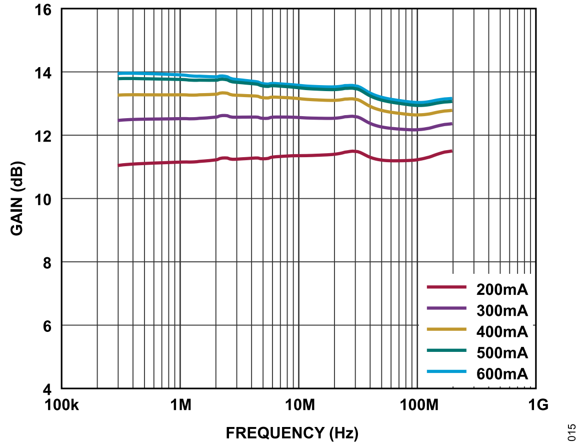


Figure 15. Gain vs. Frequency for Various I_{DQ} Values, 300 kHz to 200 MHz, V_{DD} = 15 V

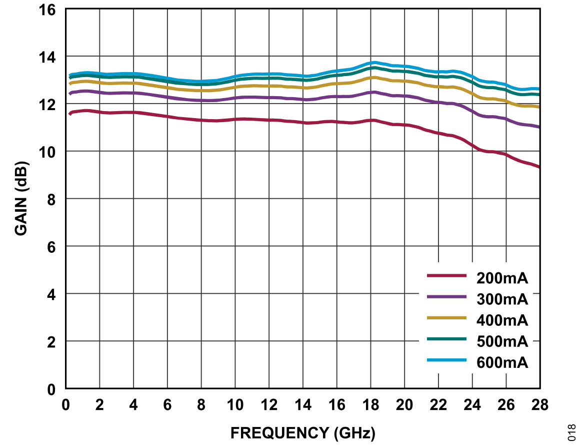


Figure 18. Gain vs. Frequency for Various I_{DQ} Values, 200 MHz to 28 GHz, V_{DD} = 15 V

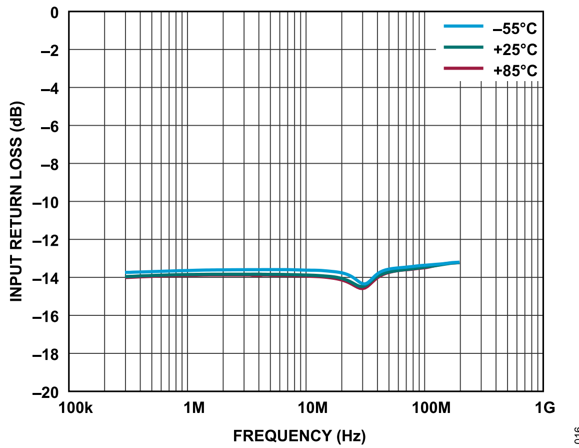


Figure 16. Input Return Loss vs. Frequency for Various Temperatures, 300 kHz to 200 MHz, V_{DD} = 15 V, I_{DQ} = 500 mA

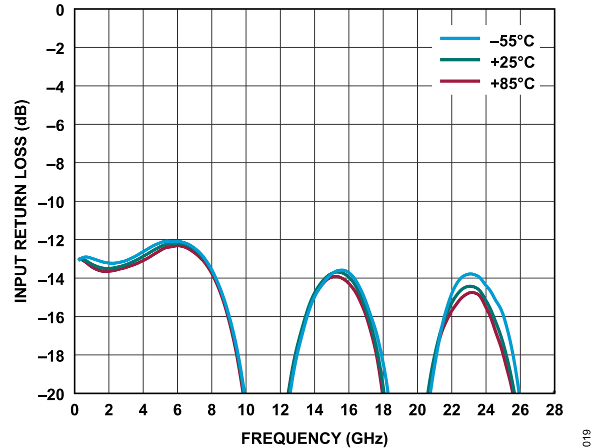


Figure 19. Input Return Loss vs. Frequency for Various Temperatures, 200 MHz to 28 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

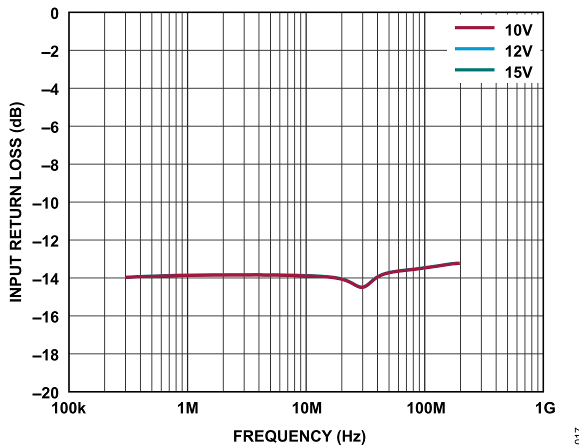


Figure 17. Input Return Loss vs. Frequency for Various V_{DD} Values, 300 kHz to 200 MHz, I_{DQ} = 500 mA

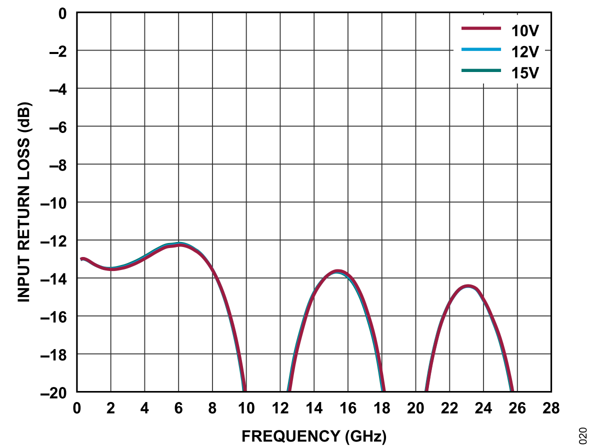


Figure 20. Input Return Loss vs. Frequency for Various V_{DD} Values, 200 MHz to 28 GHz, I_{DQ} = 500 mA

TYPICAL PERFORMANCE CHARACTERISTICS

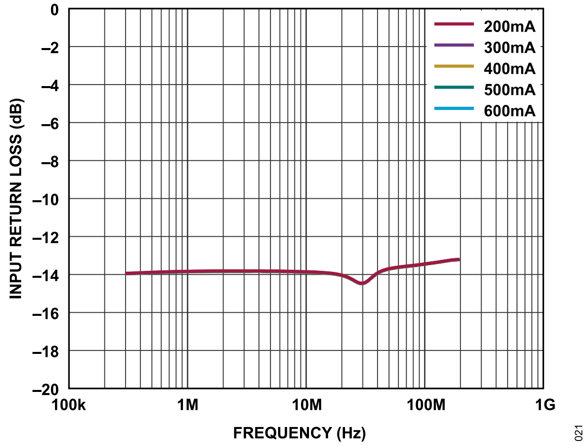


Figure 21. Input Return Loss vs. Frequency for Various I_{DQ} Values, 300 kHz to 200 MHz, V_{DD} = 15 V

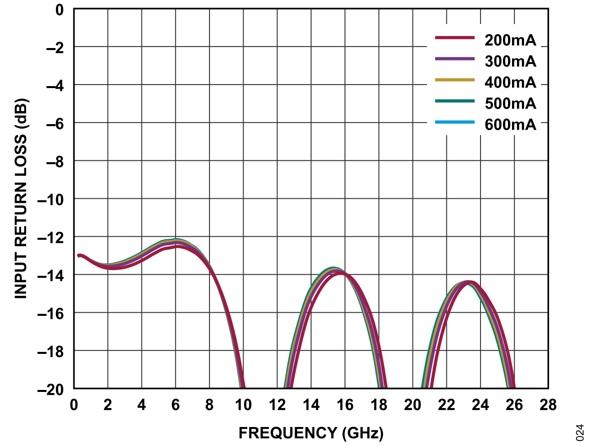


Figure 24. Input Return Loss vs. Frequency for Various I_{DQ} Values, 200 MHz to 28 GHz, V_{DD} = 15 V

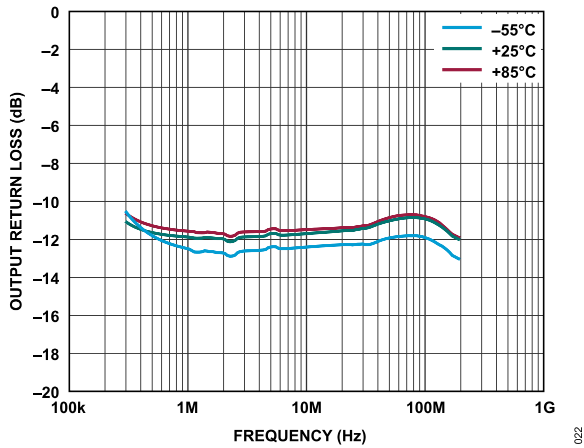


Figure 22. Output Return Loss vs. Frequency for Various Temperatures, 300 kHz to 200 MHz, V_{DD} = 15 V, I_{DQ} = 500 mA

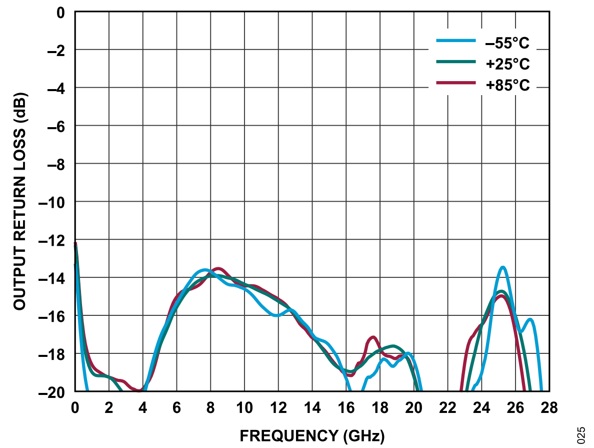


Figure 25. Output Return Loss vs. Frequency for Various Temperatures, 200 MHz to 28 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

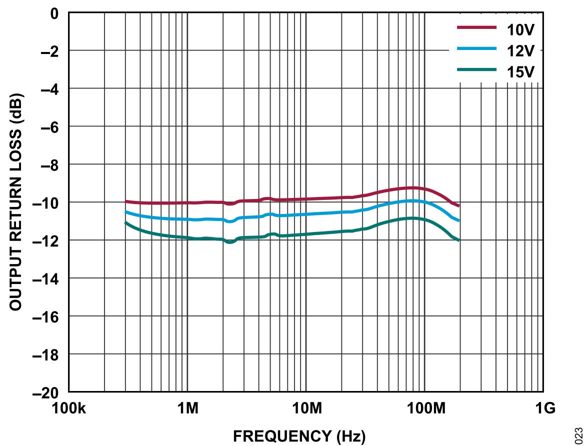


Figure 23. Output Return Loss vs. Frequency for Various V_{DD} Values, 300 kHz to 200 MHz, I_{DQ} = 500 mA

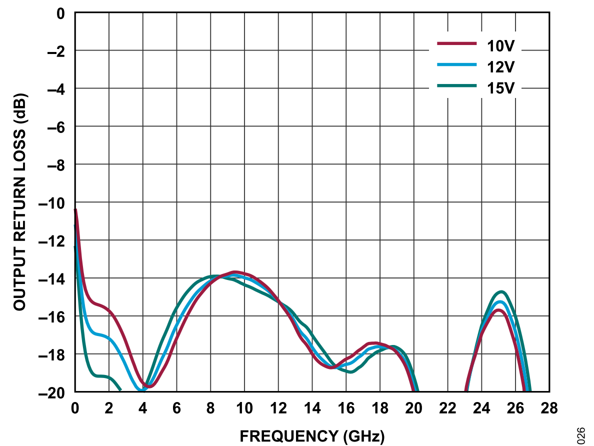


Figure 26. Output Return Loss vs. Frequency for Various V_{DD} Values, 200 MHz to 28 GHz, I_{DQ} = 500 mA

TYPICAL PERFORMANCE CHARACTERISTICS

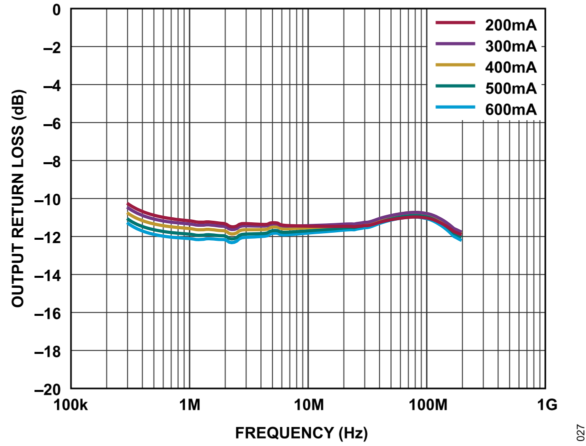


Figure 27. Output Return Loss vs. Frequency for Various I_{DQ} Values, 300 kHz to 200 MHz, V_{DD} = 15 V

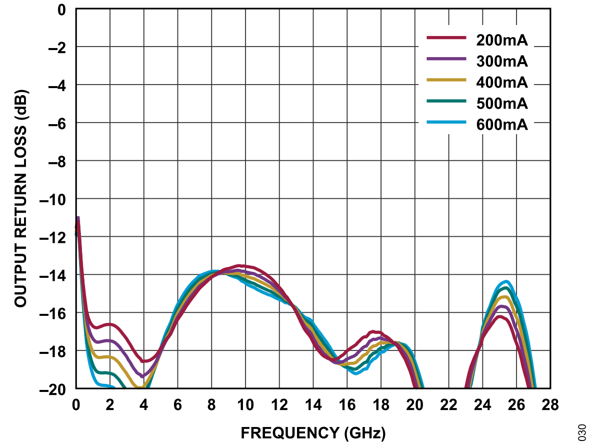


Figure 30. Output Return Loss vs. Frequency for Various I_{DQ} Values, 200 MHz to 28 GHz, V_{DD} = 15 V

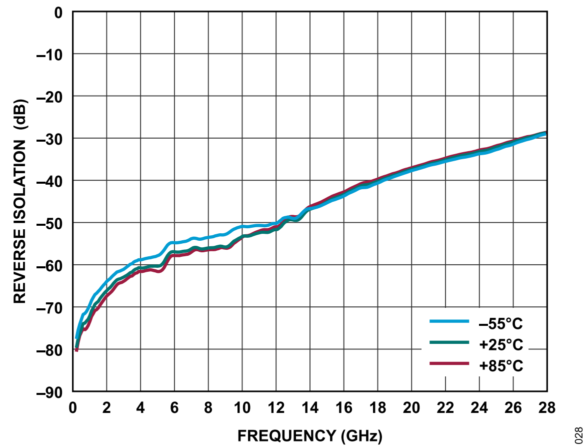


Figure 28. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 15 V, I_{DQ} = 500 mA

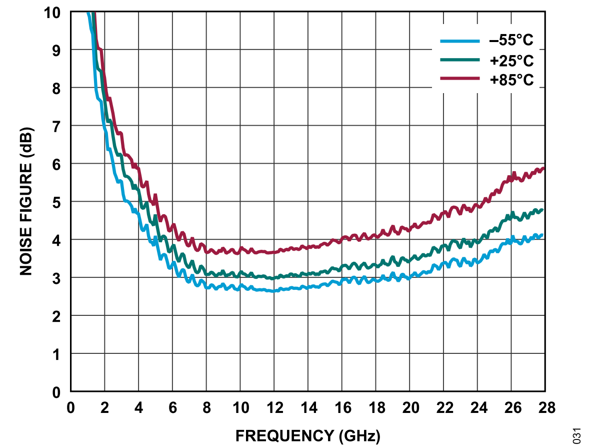


Figure 31. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 15 V, I_{DQ} = 500 mA

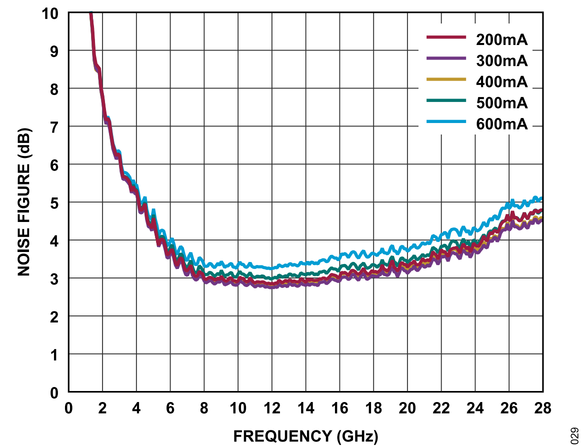


Figure 29. Noise Figure vs. Frequency for Various I_{DQ} Values, V_{DD} = 15 V

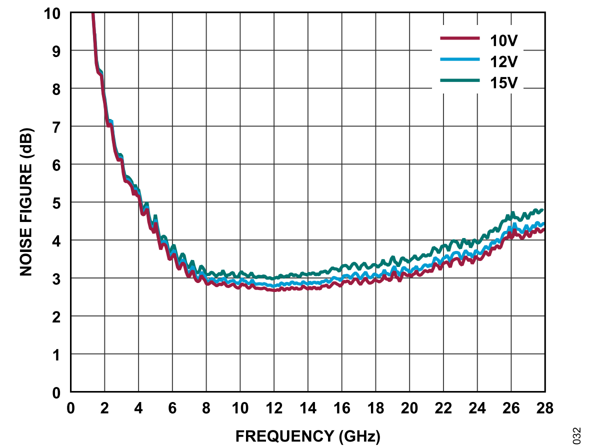


Figure 32. Noise Figure vs. Frequency for Various V_{DD} Values, I_{DQ} = 500 mA

TYPICAL PERFORMANCE CHARACTERISTICS

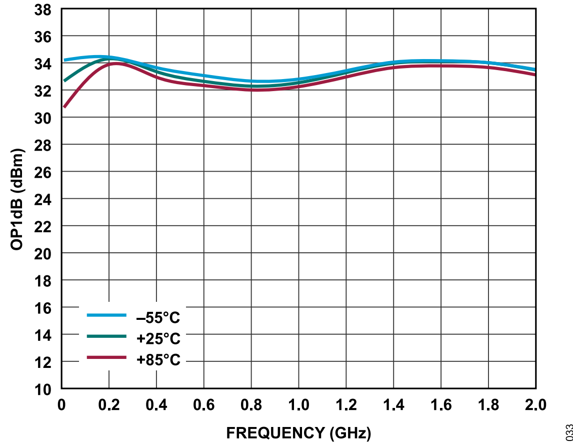


Figure 33. OP1dB vs. Frequency for Various Temperatures, 10 MHz to 2 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

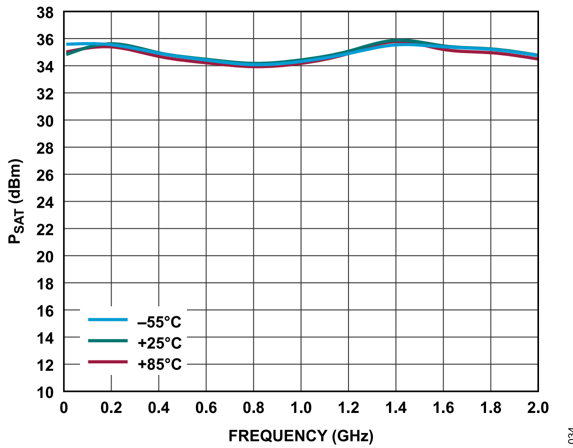


Figure 34. P_{SAT} vs. Frequency for Various Temperatures, 10 MHz to 2 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

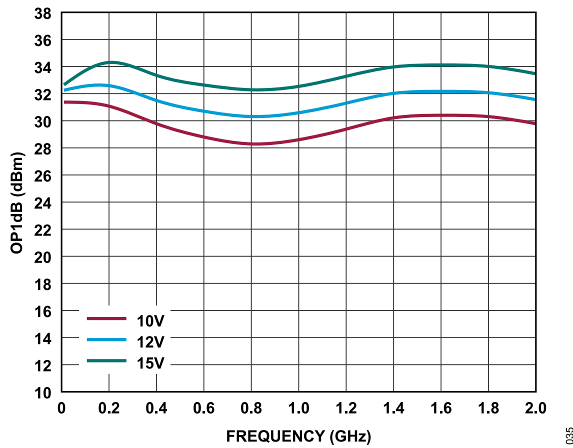


Figure 35. OP1dB vs. Frequency for Various V_{DD} Values, 10 MHz to 2 GHz, I_{DQ} = 500 mA

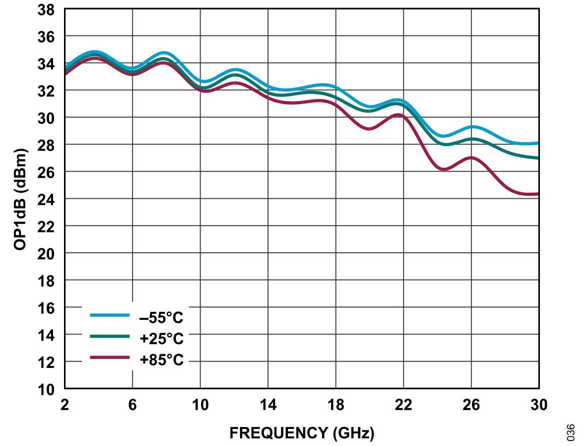


Figure 36. OP1dB vs. Frequency for Various Temperatures, 2 GHz to 30 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

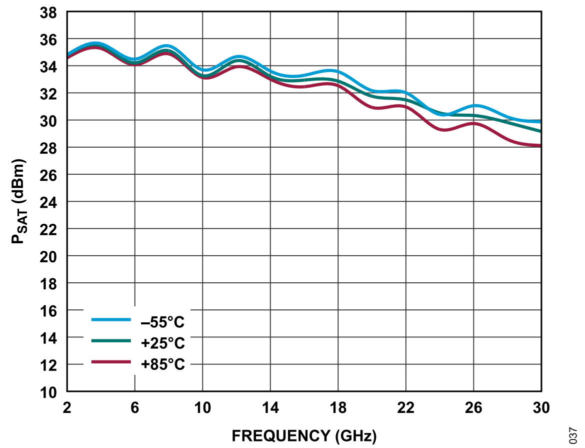


Figure 37. P_{SAT} vs. Frequency for Various Temperatures, 2 GHz to 30 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

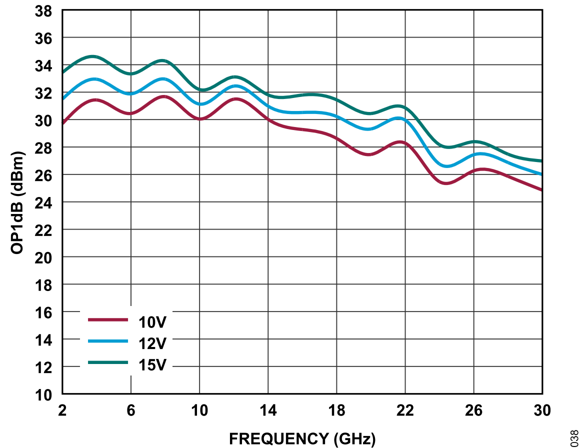


Figure 38. OP1dB vs. Frequency for Various V_{DD} Values, 2 GHz to 30 GHz, I_{DQ} = 500 mA

TYPICAL PERFORMANCE CHARACTERISTICS

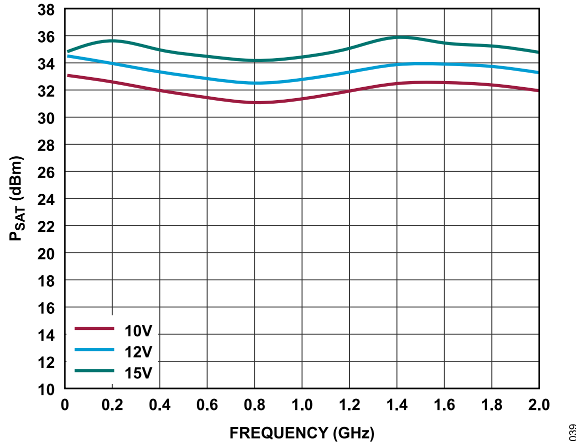


Figure 39. P_{SAT} vs. Frequency for Various V_{DD} Values, 10 MHz to 2 GHz, I_{DQ} = 500 mA

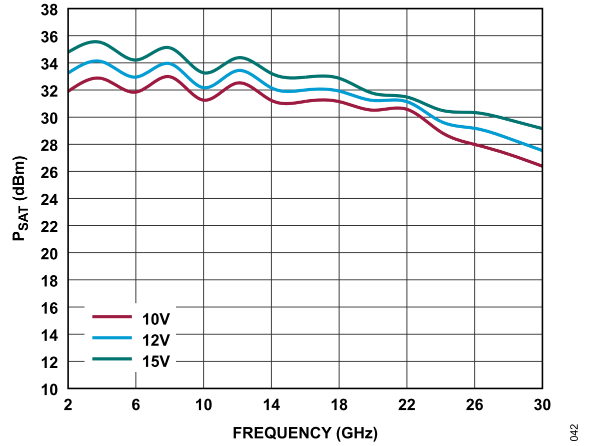


Figure 42. P_{SAT} vs. Frequency for Various V_{DD} Values, 2 GHz to 30 GHz, I_{DQ} = 500 mA

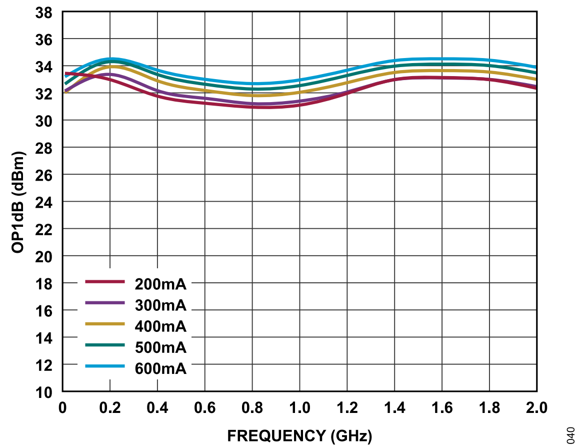


Figure 40. OP1dB vs. Frequency for Various I_{DQ} Values, 10 MHz to 2 GHz, V_{DD} = 15 V

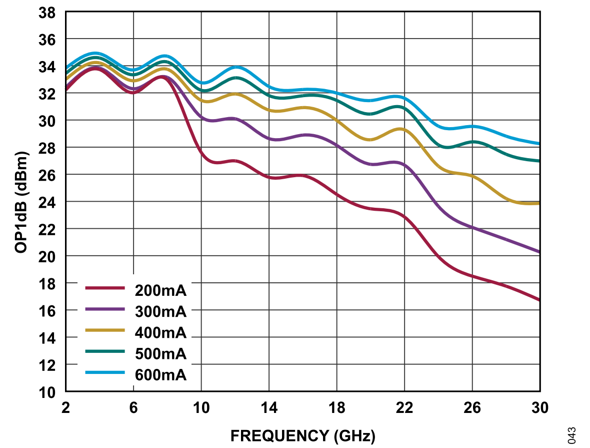


Figure 43. OP1dB vs. Frequency for Various I_{DQ} Values, 2 GHz to 30 GHz, V_{DD} = 15 V

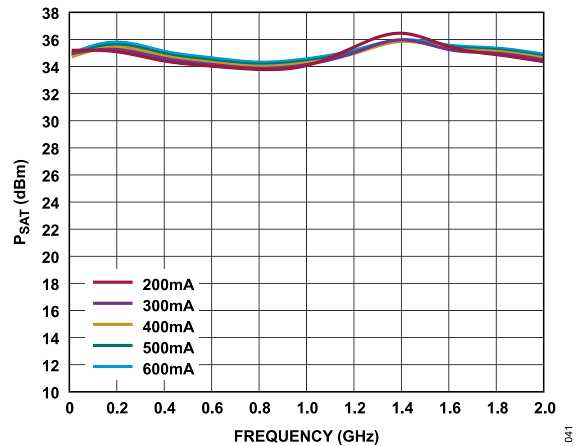


Figure 41. P_{SAT} vs. Frequency for Various I_{DQ} Values, 10 MHz to 2 GHz, V_{DD} = 15 V

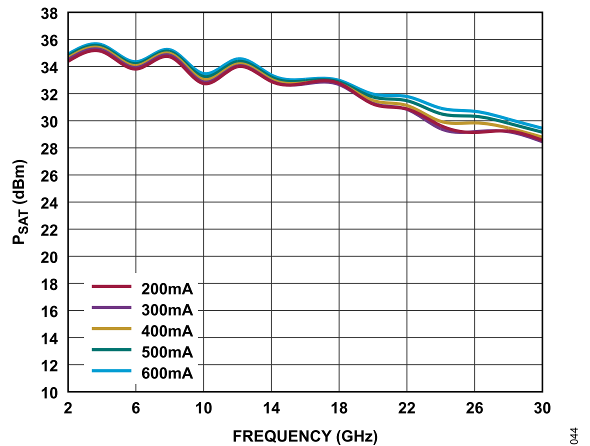


Figure 44. P_{SAT} vs. Frequency for Various I_{DQ} Values, 2 GHz to 30 GHz, V_{DD} = 15 V

TYPICAL PERFORMANCE CHARACTERISTICS

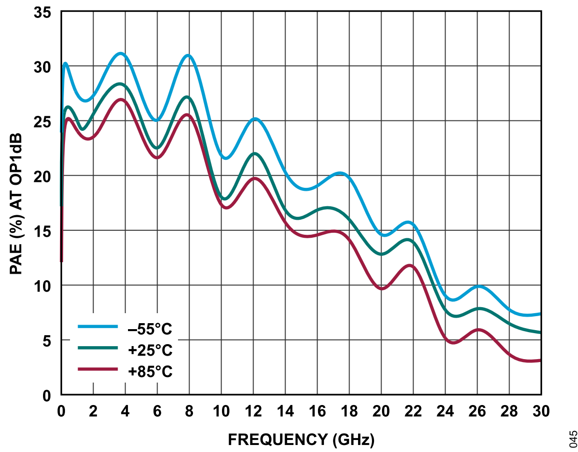


Figure 45. Power-Added Efficiency (PAE) at OP1dB vs. Frequency for Various Temperatures, V_{DD} = 15 V, I_{DQ} = 500 mA

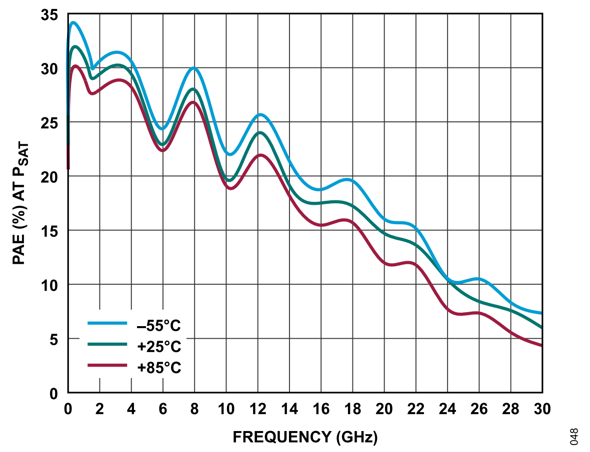


Figure 48. PAE at P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 15 V, I_{DQ} = 500 mA

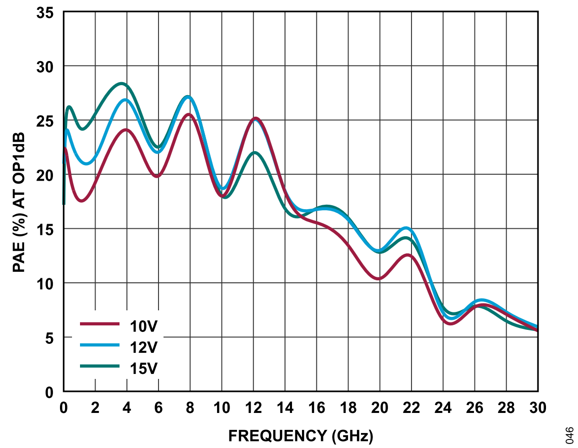


Figure 46. PAE at OP1dB vs. Frequency for Various V_{DD} Values, I_{DQ} = 500 mA

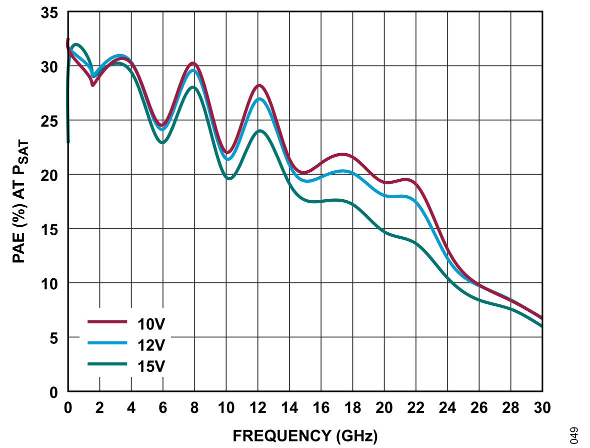


Figure 49. PAE at P_{SAT} vs. Frequency for Various V_{DD} Values, I_{DQ} = 500 mA

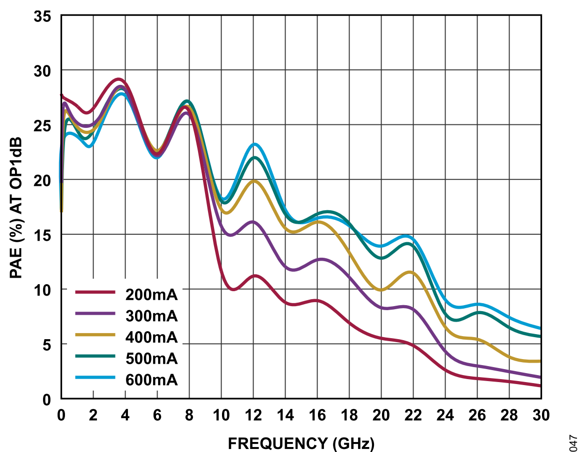


Figure 47. PAE at OP1dB vs. Frequency for Various I_{DQ} Values, V_{DD} = 15 V

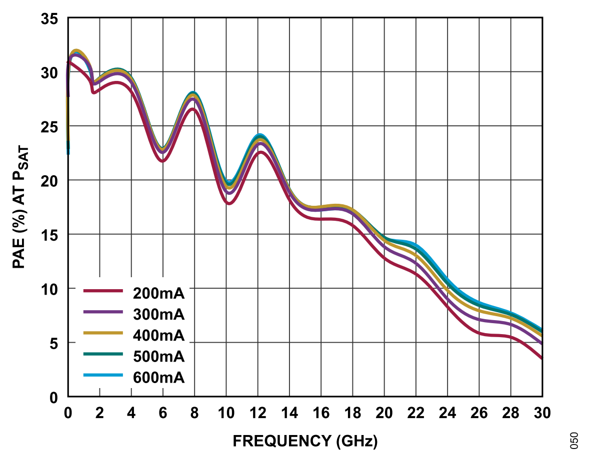


Figure 50. PAE at P_{SAT} vs. Frequency for Various I_{DQ} Values, V_{DD} = 15 V

TYPICAL PERFORMANCE CHARACTERISTICS

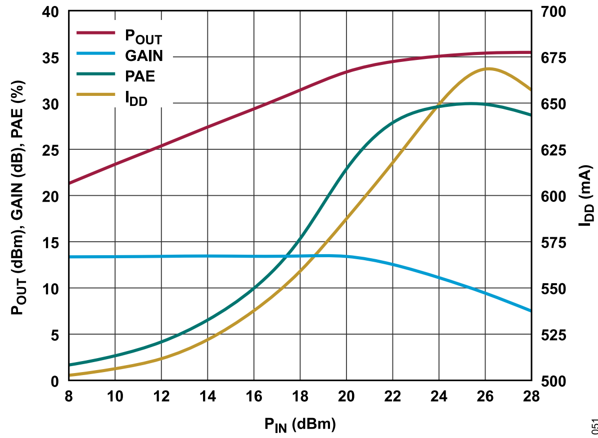


Figure 51. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 4 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

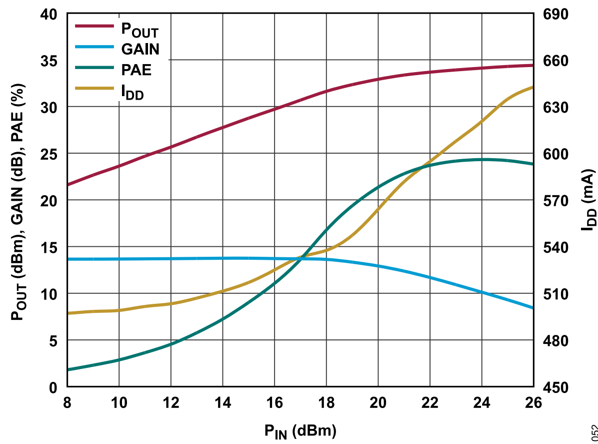


Figure 52. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 12 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

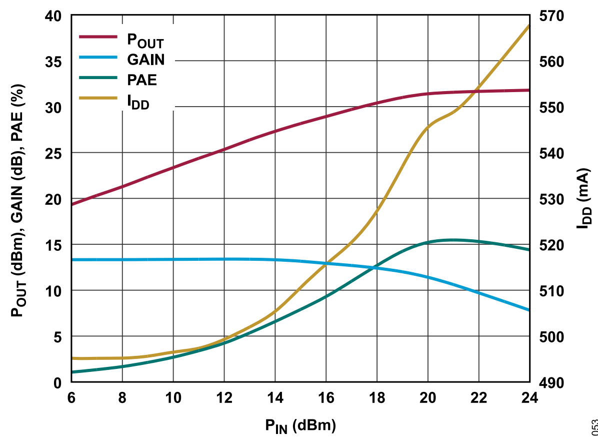


Figure 53. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 20 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

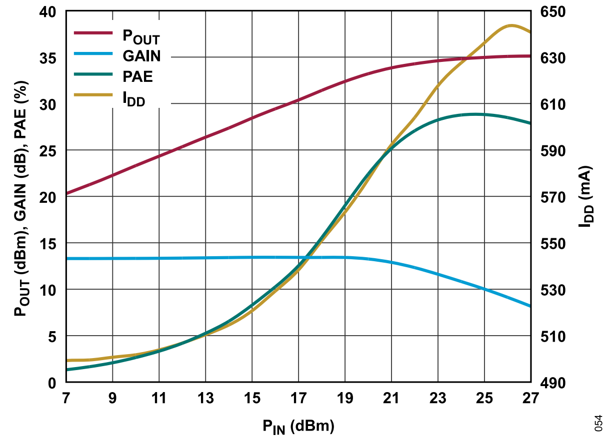


Figure 54. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 8 GHz, V_{DD} = 15 V, I_{DQ}= 500 mA

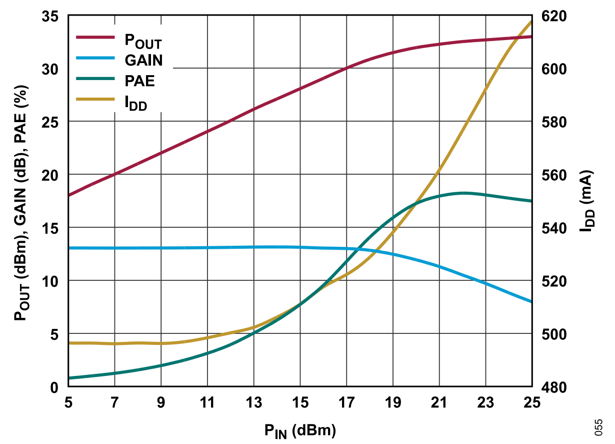


Figure 55. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 16 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

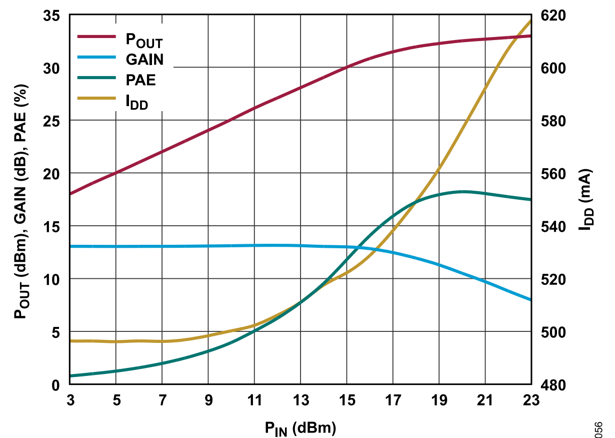


Figure 56. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 24 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

TYPICAL PERFORMANCE CHARACTERISTICS

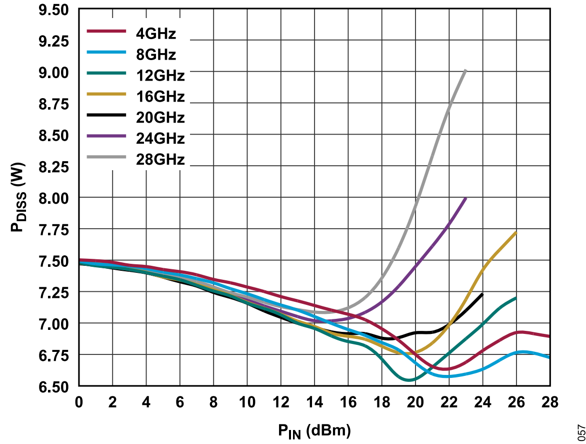


Figure 57. P_{DISS} vs. P_{IN} for Various Frequencies at T_{CASE} = 85°C, V_{DD} = 15 V, I_{DQ} = 500 mA

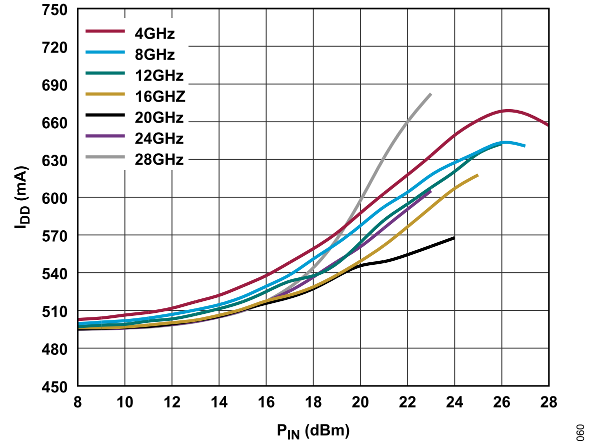


Figure 60. I_{DD} vs. P_{IN} for Various Frequencies, V_{DD} = 15 V, I_{DQ} = 500 mA

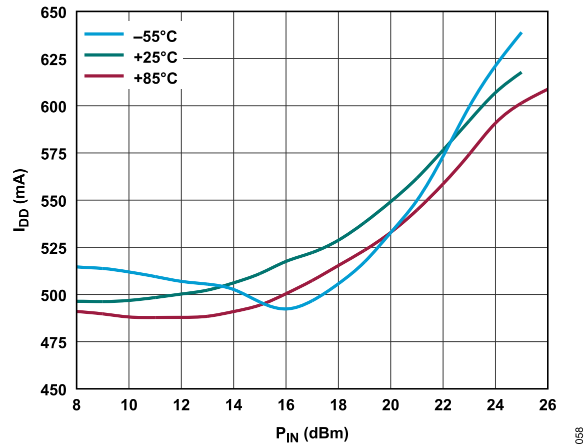


Figure 58. I_{DD} vs. P_{IN} for Various Temperatures, 16 GHz, V_{DD} = 15 V, I_{DQ} = 500 mA

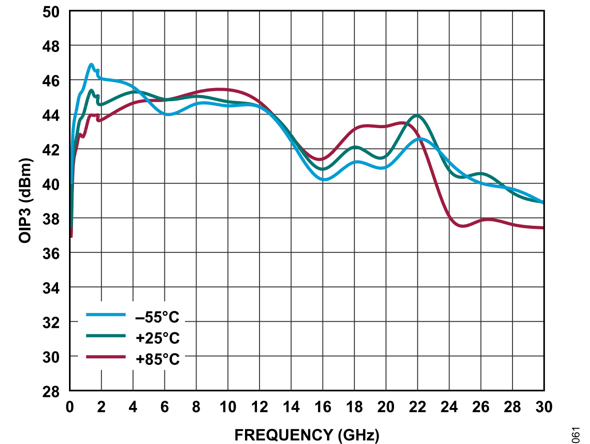


Figure 61. OIP3 vs. Frequency for Various Temperatures, 50 MHz to 30 GHz, P_{OUT} per Tone = 16 dBm, V_{DD} = 15 V, I_{DQ} = 500 mA

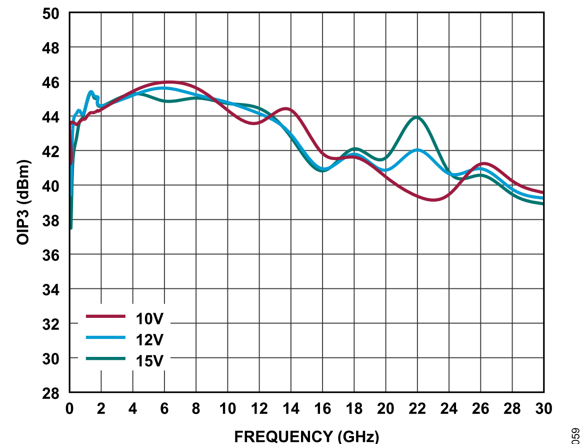


Figure 59. OIP3 vs. Frequency for Various V_{DD} Values, 50 MHz to 30 GHz, P_{OUT} per Tone = 16 dBm, I_{DQ} = 500 mA

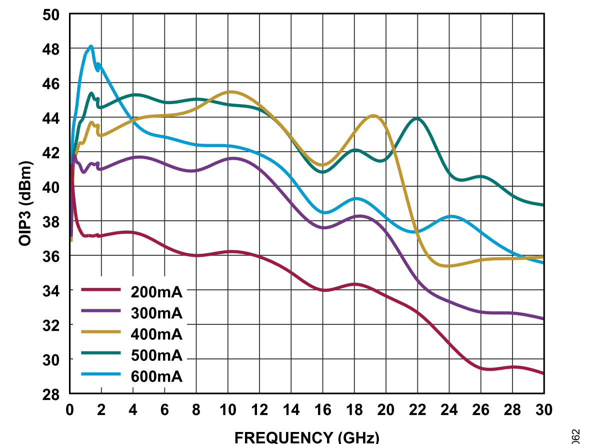


Figure 62. OIP3 vs. Frequency for Various I_{DQ} Values, 50 MHz to 30 GHz P_{OUT} per Tone = 16 dBm, V_{DD} = 15 V

TYPICAL PERFORMANCE CHARACTERISTICS

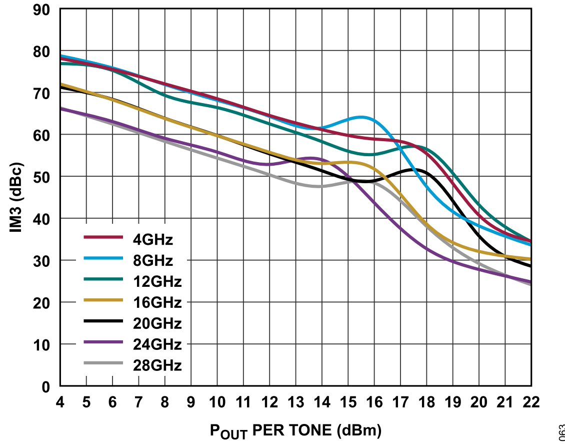


Figure 63. Third-Order Intermodulation Distortion (IM3) vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 10 V, I_{DQ} = 500 mA

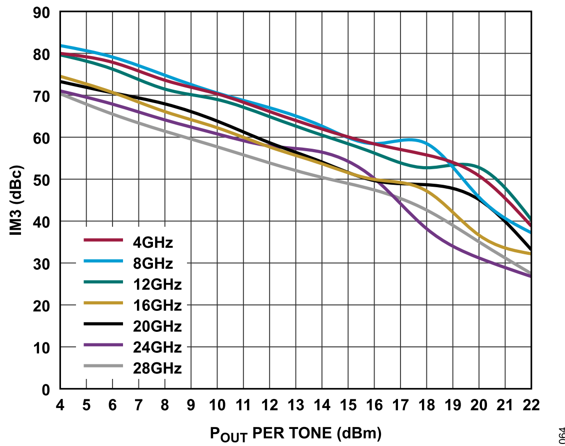


Figure 64. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 12 V, I_{DQ} = 500 mA

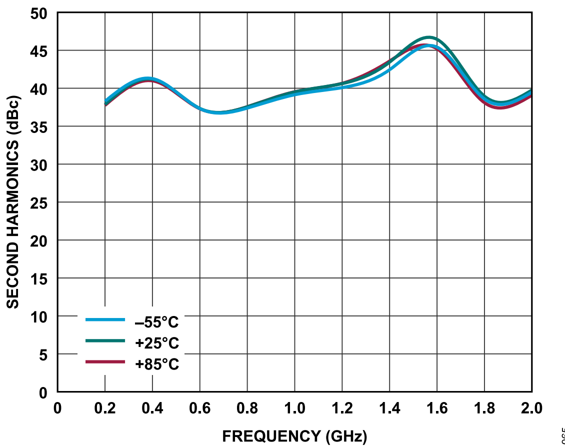


Figure 65. Low Frequency Second Harmonics vs. Frequency for Various Temperatures, V_{DD} = 15 V, I_{DQ} = 500 mA, P_{OUT} = 16 dBm

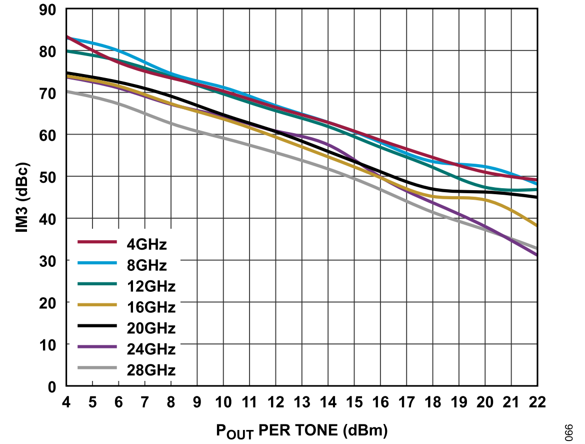


Figure 66. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 15 V, I_{DQ} = 500 mA

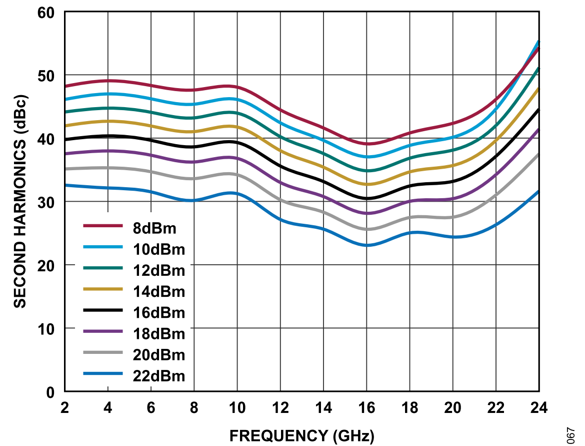


Figure 67. Second Harmonics vs. Frequency for Various P_{OUT} Values, V_{DD} = 15 V, I_{DQ} = 500 mA

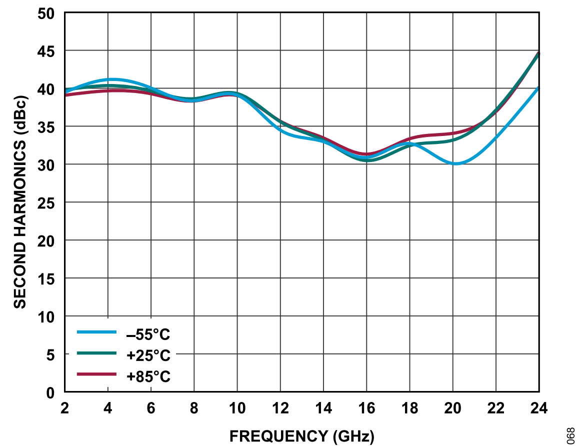


Figure 68. Second Harmonics vs. Frequency for Various Temperatures, V_{DD} = 15 V, I_{DQ} = 500 mA, P_{OUT} = 16 dBm

TYPICAL PERFORMANCE CHARACTERISTICS

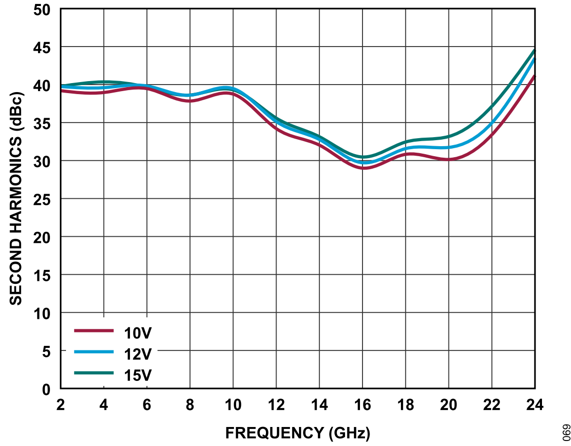


Figure 69. Second Harmonics vs. Frequency for Various V_{DD} Values, I_{DQ} = 500 mA, P_{OUT} = 16 dBm

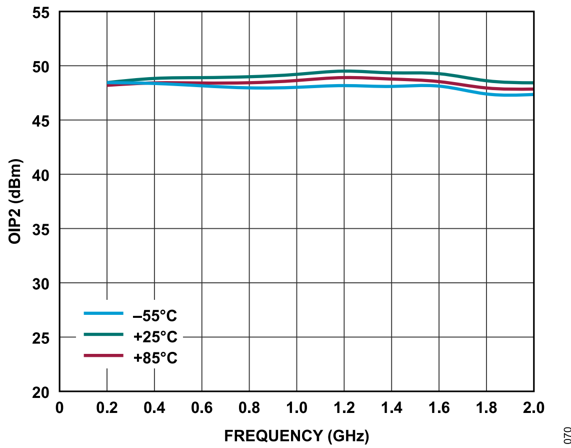


Figure 70. Low Frequency OIP2 vs. Frequency for Various Temperatures, V_{DD} = 15 V, I_{DQ} = 500 mA, P_{OUT} = 16 dBm

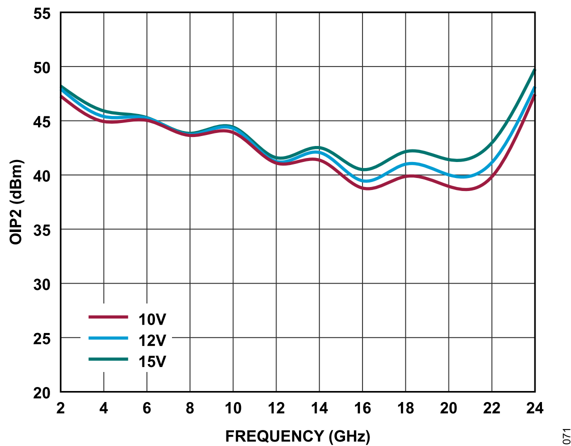


Figure 71. OIP2 vs. Frequency for Various V_{DD} Values, I_{DQ} = 500 mA, P_{OUT} = 16 dBm

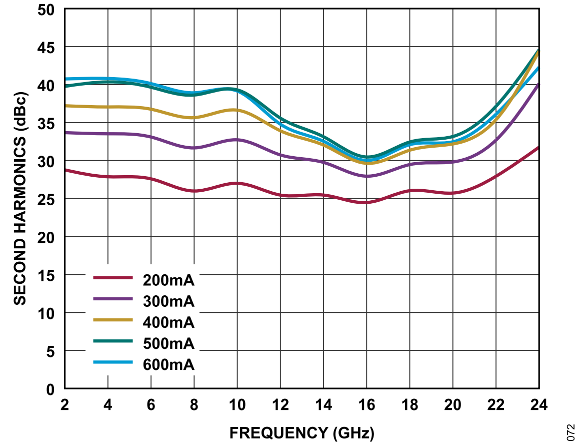


Figure 72. Second Harmonics vs. Frequency for Various I_{DQ} Values, V_{DD} = 15 V, P_{OUT} = 16 dBm

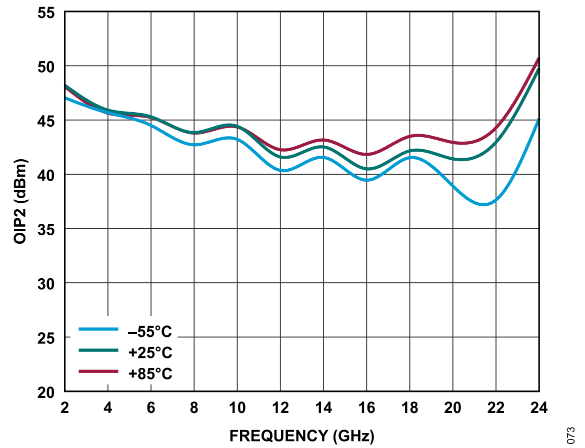


Figure 73. OIP2 vs. Frequency for Various Temperatures, V_{DD} = 15 V, I_{DQ} = 500 mA, P_{OUT} = 16 dBm

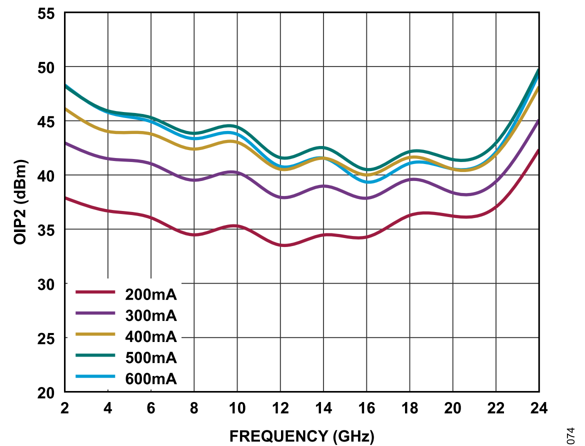


Figure 74. OIP2 vs. Frequency for Various I_{DQ} Values, V_{DD} = 15 V, P_{OUT} = 16 dBm

TYPICAL PERFORMANCE CHARACTERISTICS

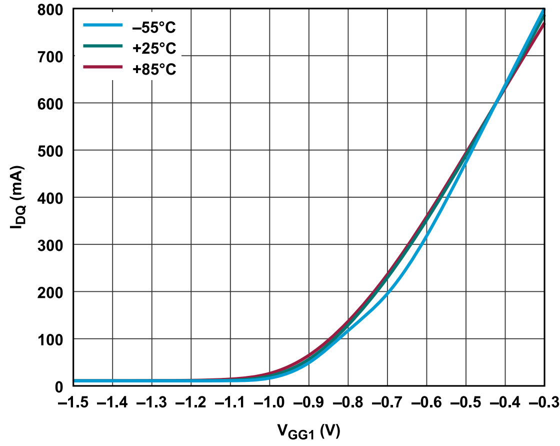


Figure 75. I_{DQ} vs. V_{GG1} for Various Temperatures, V_{DD} = 15 V

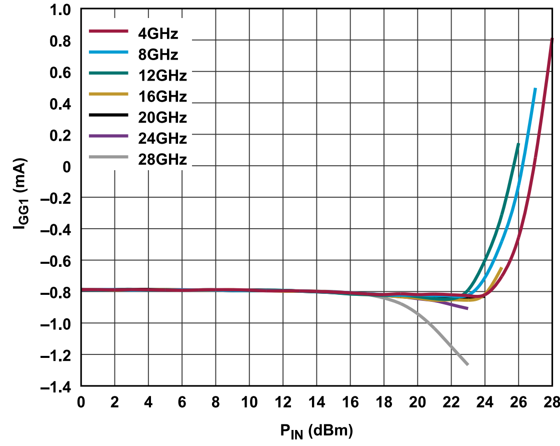


Figure 78. I_{GG1} vs. P_{IN} for Various Frequencies, V_{DD} = 15 V

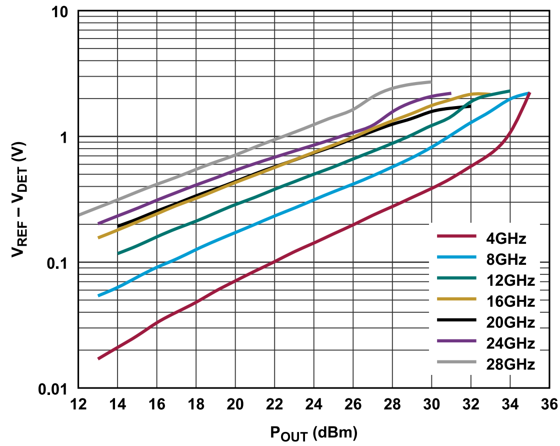


Figure 76. Detector Voltage (V_{REF} − V_{DET}) vs. P_{OUT} for Various Frequencies

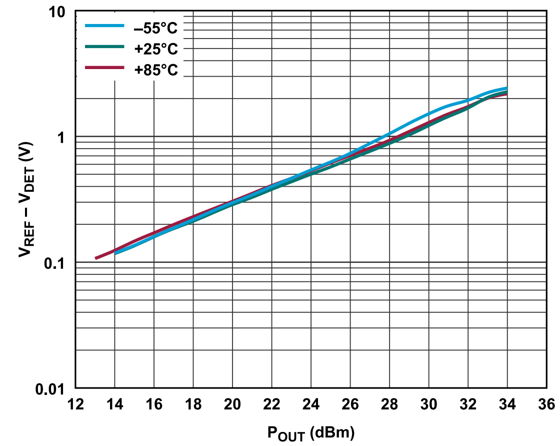


Figure 79. V_{REF} − V_{DET} vs. P_{OUT} for Various Temperatures at 12 GHz

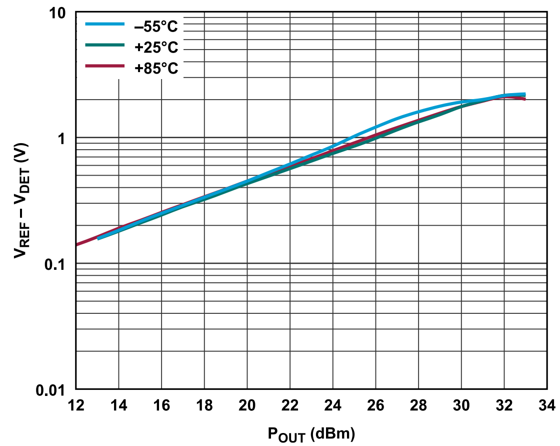


Figure 77. V_{REF} − V_{DET} vs. P_{OUT} for Various Temperatures at 16 GHz

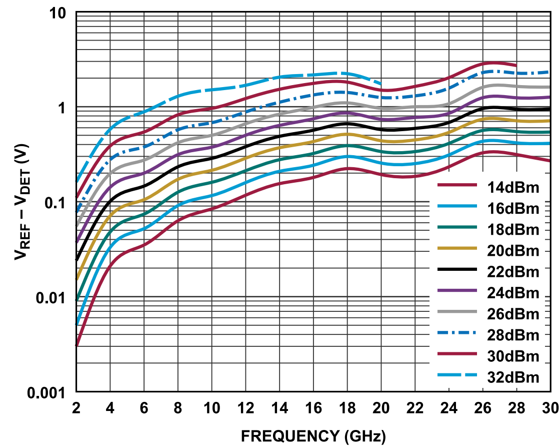


Figure 80. V_{REF} − V_{DET} vs. Frequency for Various P_{OUT} Values

TYPICAL PERFORMANCE CHARACTERISTICS

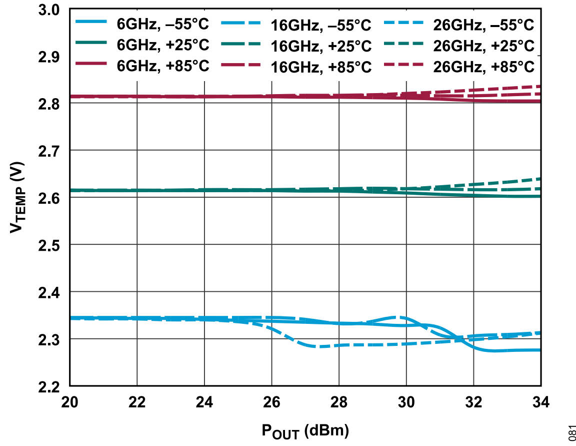


Figure 81. Temperature Sensor Voltage (V_{TEMP}) vs. P_{OUT} for Various Frequencies and Temperatures, V_{DD} = 15 V, I_{DQ} = 500 mA, VBTEMP Voltage (VB_{TEMP}) = 5 V

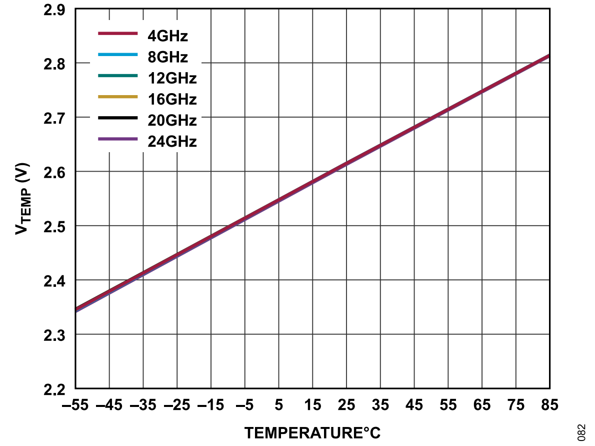


Figure 82. V_{TEMP} vs. Temperature for Various Frequencies, P_{OUT} = 22 dBm, V_{DD} = 15 V, I_{DQ} = 500 mA, VB_{TEMP} = 5 V

THEORY OF OPERATION

The ADPA9007-2CHIP is a broadband distributed GaAs, pHEMT, medium power amplifier. The simplified block diagram is shown in Figure 83. The drain current is set by a negative voltage (−1.5 V to 0 V) applied to the gate pad, VGG1. For an I_{DQ} of 500 mA, a gate bias voltage of −0.6 V is typically required. The drain bias voltage is applied through the RFOUT/VDD pad via a broadband bias tee or external bias network.

A portion of the RF output signal is directionally coupled to a diode for detection of the RF output power. When the diode is DC biased, the diode rectifies the RF power and makes it available for measurement as a DC voltage at the VDET pad. To allow temperature compensation of V_{DET}, an identical circuit (minus the coupled RF power) is available via the VREF pad. Taking the difference of $V_{REF} - V_{DET}$ provides a temperature compensated signal that is proportional to the RF output power.

The ADPA9007-2CHIP contains an integrated temperature sensor. With a DC bias voltage applied to the VBTEMP pad of the temperature sensor, a voltage proportional to the device temperature is available on the VTEMP pad.

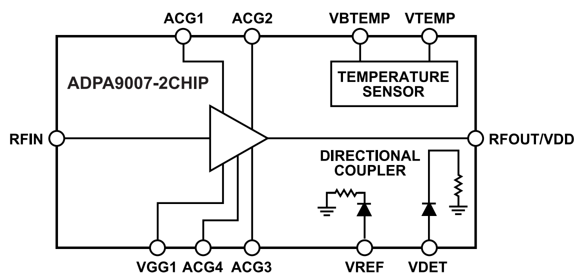


Figure 83. ADPA9007-2CHIP Simplified Block Diagram

APPLICATIONS INFORMATION

The basic connections for operating the ADPA9007-2CHIP are shown in Figure 84. The RFIN and the RFOUT/VDD pads require external AC-coupling capacitors. The drain bias (V_{DD}) is applied through a bias tee on the RFOUT/VDD pad. The nominal drain bias is 15 V. The negative gate current is applied to the VGG1 pad. A V_{GG1} of approximately −0.6 V sets the drain current to 500 mA.

The VDET and VREF pads are connected to 5 V through 40.2 kΩ biasing resistors to bias internal circuits. Figure 84 shows an optional op amp differential amplifier circuit that can be used to subtract V_{DET} from V_{REF}, yielding a temperature-compensated voltage that is proportional to the RF output power.

The configuration shown in Figure 84 was used to characterize the device with the exception of the op amp circuit. V_{DET} and V_{REF} were measured at their respective pads with only the two 40.2 kΩ biasing resistors attached.

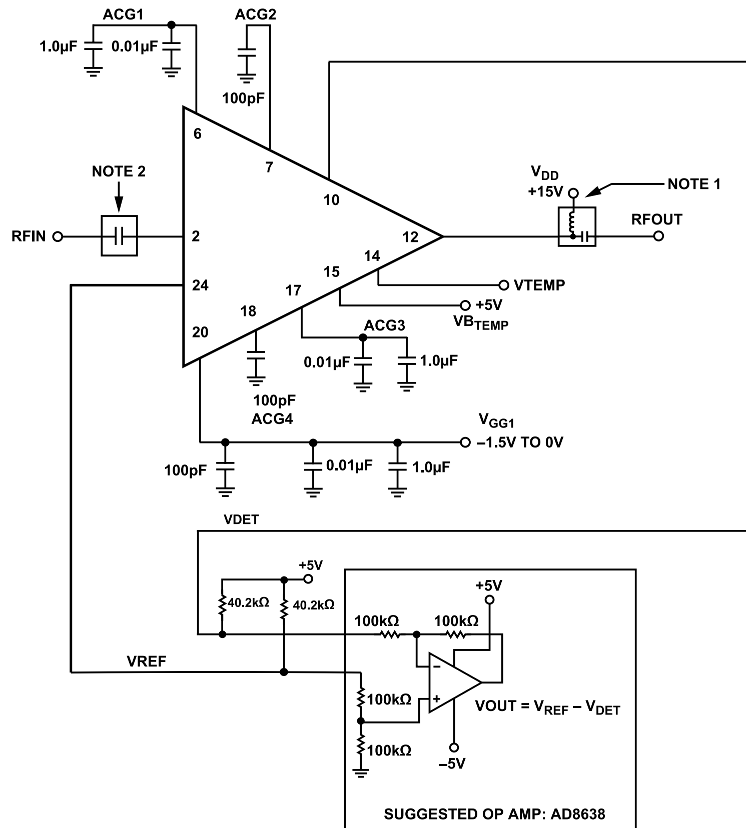


Figure 84. Basic Connections

APPLICATIONS INFORMATION

POWER-UP SEQUENCE

The following power-up sequence is recommended:

1. Connect the power supply grounds to GND.
2. Set V_{GG1} to −1.5 V.
3. Set RFOUT/VDD to 15 V.
4. Increase V_{GG1} to achieve an I_{DQ} of 500 mA, approximately −0.6 V.
5. Apply the RF signal.

POWER-DOWN SEQUENCE

The following power-down sequence is recommended:

1. Turn off the RF signal.
2. Decrease V_{GG1} to −1.5 V to achieve an I_{DQ} of 0 mA.
3. Decrease the voltage on V_{DD} to 0 V.
4. Increase V_{GG1} to 0 V.

BIASING THE ADPA9007-2CHIP WITH THE HMC980LP4E

The HMC980LP4E is an active bias controller that is designed to meet the bias requirements for enhancement mode and depletion mode amplifiers, such as the ADPA9007-2CHIP. Refer to the ADPA9007 packaged device data sheet for guidance on how to configure the HMC980LP4E to control ADPA9007-2CHIP.

ASSEMBLY DIAGRAM

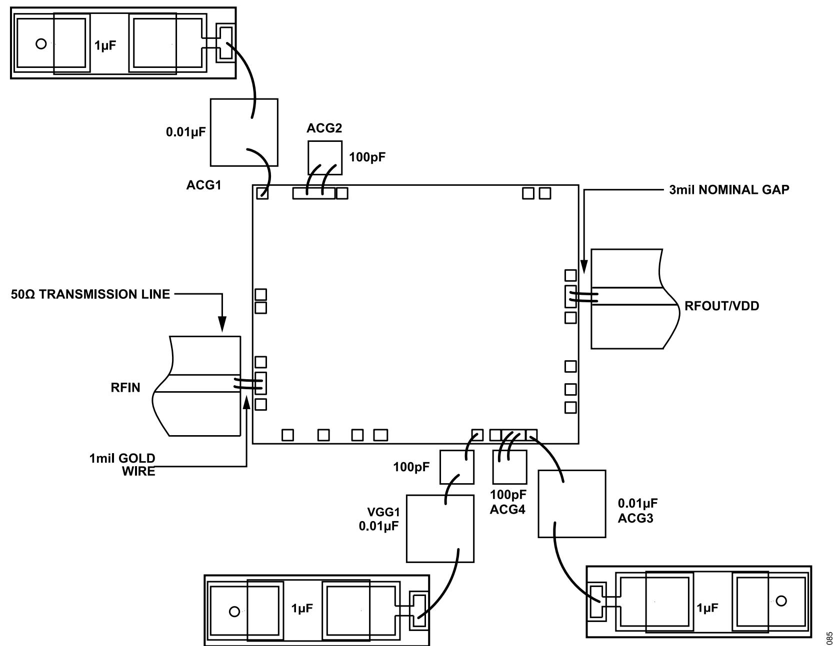


Figure 85. Assembly Diagram

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE, GAAS, MMICS

Attach the die directly to the ground plane with high thermal conductive epoxy (see the Handling Precautions section, the Mounting section, and the Wire Bonding section).

Place the microstrip substrates as close to the die as possible to minimize wire bond length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

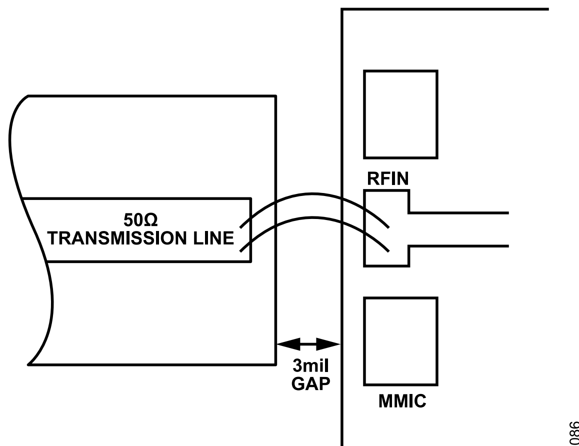


Figure 86. Input Wire Bonding and Substrate Spacing

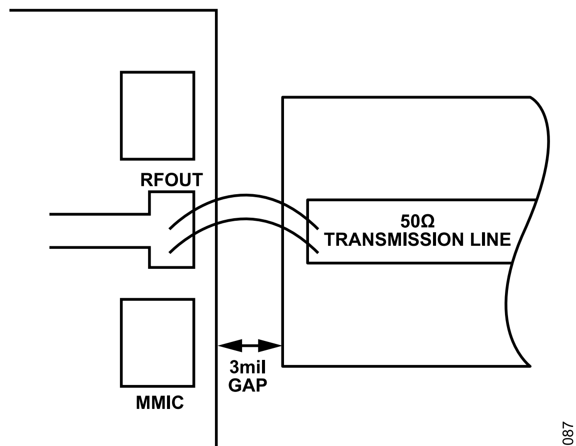


Figure 87. Output Wire Bonding and Substrate Spacing

Handling Precautions

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle- or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all dies in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of tweezers. The surface of the chip has fragile air bridges and must not be touched with a vacuum collet, tweezers, or fingers.

Mounting

Before the die is attached, apply enough epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Cure the epoxy per the schedule of the manufacturer.

Wire Bonding

RF bonds made with 1 mil gold wire are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. Thermosonically bonded DC bonds of 0.025 mm diameter (0.001 in) are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply the minimum amount of ultrasonic energy (depending on the process and package being used) to achieve reliable bonds. Keep all bonds as short as possible, less than 0.31 mm (12 mil).

OUTLINE DIMENSIONS

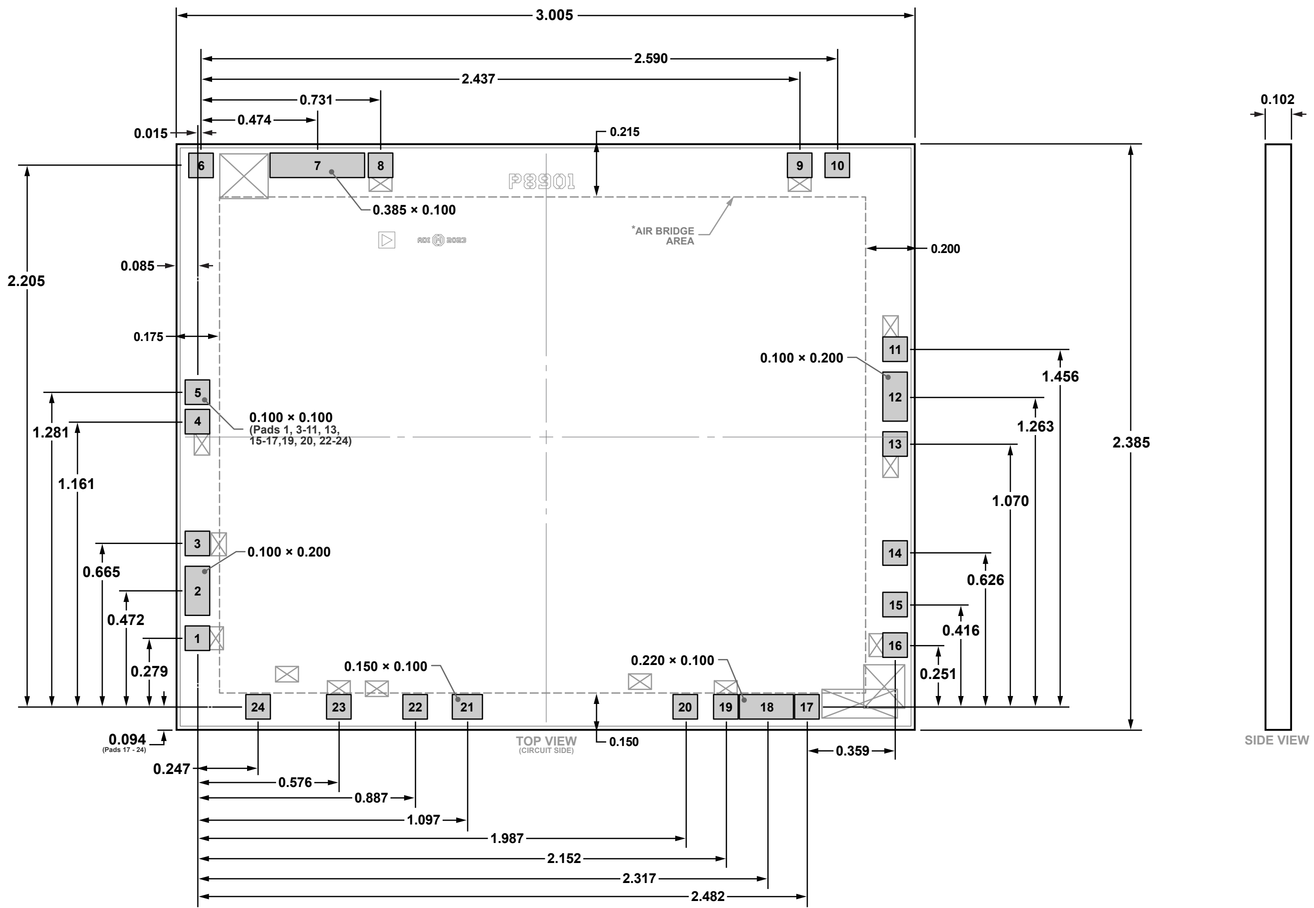


Figure 88. 24-Pad Bare Die [CHIP]
(C-24-7)
Dimensions shown in millimeters

Updated: August 11, 2023

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADPA9007-2CHIP	−55°C to +85°C	24-Pad Bare Die [CHIP]	C-24-7
ADPA9007-2C-SX	−55°C to +85°C	24-Pad Bare Die [CHIP]	C-24-7

1 The ADPA9007-2CHIP and ADPA9007-2C-SX are RoHS-compliant parts.

2 These models have been visually inspected to MIL-STD-883.

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