

10 kHz to 22 GHz, Ultrawideband, Low Noise Amplifier

FEATURES

- ▶ Wideband operation: 10 kHz to 22 GHz
- ▶ Single positive supply (self biased) typical: 5 V and 90 mA
- ▶ R_{BIAS} drain current adjustment pin
- ▶ Gain: 14 dB typical from 10 kHz to 16 GHz
- ▶ Noise figure: 3.5 dB typical from 10 kHz to 16 GHz
- ▶ Extended operating temperature range: -55°C to $+125^{\circ}\text{C}$
- ▶ RoHS-compliant, 2 mm × 2 mm, 8-lead lead frame chip scale package [LFCSP]

APPLICATIONS

- ▶ Telecommunications
- ▶ Instrumentation
- ▶ Radar
- ▶ Electronic warfare

GENERAL DESCRIPTION

The ADL8101 is an ultrawideband low noise amplifier (LNA) that operates from 10 kHz to 22 GHz. The typical gain and noise figure are 14 dB and 3.5 dB, respectively, from 10 kHz to 16 GHz. The output power for 1 dB compression (OP1dB), output third-order intercept (OIP3), and output second-order intercept (OIP2) are 15 dBm, 26 dBm, and 29 dBm, respectively, from 10 kHz to 16 GHz. The nominal quiescent current (I_{DQ}), which can be adjusted, is 90 mA from a 5 V supply voltage (V_{DD}). The internally matched, DC-coupled RF input and output pins require external AC coupling capacitors along with a bias inductor on RFOUT.

The ADL8101 is fabricated on a pseudomorphic high electron mobility transistor (pHEMT) process. It is housed in an [RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP](#) and is specified for operation from -55°C to $+125^{\circ}\text{C}$.

FUNCTIONAL BLOCK DIAGRAM

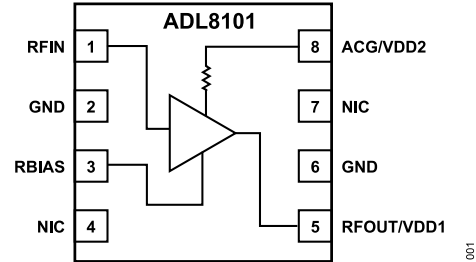


Figure 1. Functional Block Diagram

TABLE OF CONTENTS

Features.....	1	10 MHz to 22 GHz Bias Tee, Biasing	
Applications.....	1	Through the ACG/VDD2 Pin.....	20
General Description.....	1	10 kHz to 22 GHz Bias Tee.....	24
Functional Block Diagram.....	1	10 kHz to 22 GHz Bias Tee, Biasing	
Specifications.....	3	Through the ACG/VDD2 Pin.....	26
10 kHz to 16 GHz Frequency Range.....	3	Theory of Operation.....	28
16 GHz to 22 GHz Frequency Range.....	3	Applications Information.....	29
DC Specifications.....	4	Recommended Bias Sequencing.....	30
Absolute Maximum Ratings.....	5	Operation from 10 kHz to 22 GHz.....	31
Thermal Resistance.....	5	Providing Drain Bias Through the ACG/ VDD2 Pin.....	32
Electrostatic Discharge (ESD) Ratings.....	5	Overdrive Recovery Optimization.....	33
ESD Caution.....	5	Recommended Power Management Circuit.....	34
Pin Configuration and Function Descriptions.....	6	Outline Dimensions.....	35
Interface Schematics.....	6	Ordering Guide.....	35
Typical Performance Characteristics	7	Evaluation Boards.....	35
10 MHz to 22 GHz Bias Tee.....	7		

REVISION HISTORY**7/2024—Revision 0: Initial Version**

SPECIFICATIONS

10 KHZ TO 16 GHZ FREQUENCY RANGE

$V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, bias resistance (R_{BIAS}) = 715 Ω , and $T_{CASE} = 25^\circ\text{C}$, unless otherwise noted.

Table 1. 10 kHz to 16 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	0.00001		16	GHz	Refer to the 10 kHz to 22 GHz Bias Tee section for the parameter coverage and operation down to 10 kHz range
GAIN	12	14		dB	
Gain Variation over Temperature		0.0168		dB/ $^\circ\text{C}$	
NOISE FIGURE		3.5		dB	
RETURN LOSS					
Input (S11)		17		dB	
Output (S22)		17		dB	
OUTPUT					
OP1dB	13	15		dBm	
Saturated Output Power (P_{SAT})		18		dBm	
OIP3		26		dBm	Measurement taken at output power (P_{OUT}) per tone = 0 dBm
OIP2		29		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
POWER ADDED EFFICIENCY (PAE)		8.66		%	Measured at P_{SAT}

16 GHZ TO 22 GHZ FREQUENCY RANGE

$V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, $R_{BIAS} = 715\ \Omega$, and $T_{CASE} = 25^\circ\text{C}$, unless otherwise noted.

Table 2. 16 GHz to 22 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	16		22	GHz	
GAIN	12	14		dB	
Gain Variation over Temperature		0.0205		dB/ $^\circ\text{C}$	
NOISE FIGURE		3.8		dB	
RETURN LOSS					
S11		12		dB	
S22		10		dB	
OUTPUT					
OP1dB	12	14		dBm	
P_{SAT}		16.5		dBm	
OIP3		25		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
OIP2		29		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
PAE		5.83		%	Measured at P_{SAT}

SPECIFICATIONS**DC SPECIFICATIONS***Table 3. DC Specifications*

Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT				
I_{DQ} Amplifier Current (I_{DQ_AMP})		90		mA
R_{BIAS} Current (I_{RBIAS})		84.5		mA
		5.5		mA
SUPPLY VOLTAGE				
V_{DD}	3	5	6	V

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
VDD1	7 V
VDD2	11 V
RF Input Power (RFIN)	23 dBm
Continuous Power Dissipation (P_{DISS}), $T_{CASE} = 85^{\circ}\text{C}$ (Derate 15.24 mW/ $^{\circ}\text{C}$ Above 85 $^{\circ}\text{C}$)	1.37 W
Temperature Range	
Storage Range	-65 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$
Operating Range	-55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$
Quiescent Channel ($T_{CASE} = 85^{\circ}\text{C}$, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, Input Power (P_{IN}) = Off)	114.5 $^{\circ}\text{C}$
Maximum Channel	175 $^{\circ}\text{C}$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel-to-case thermal resistance.

Table 5. Thermal Resistance¹

Package Type	θ_{JC}	Unit
CP-8-30		
Quiescent, $T_{CASE} = 25^{\circ}\text{C}$	55.1	$^{\circ}\text{C}/\text{W}$
Worst Case, ² $T_{CASE} = 85^{\circ}\text{C}$	65.6	$^{\circ}\text{C}/\text{W}$

¹ Thermal resistance varies with operating conditions.

² Across all specified operating conditions.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8101

Table 6. ADL8101, 8-Lead LFCSP

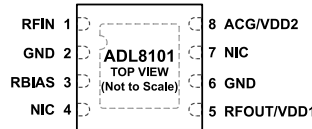
ESD Model	Withstand Threshold (V)	Class
HBM	± 250	1A

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. NIC = NO INTERNAL CONNECTION. THE NIC PIN IS NOT CONNECTED INTERNALLY. FOR NORMAL OPERATION, CONNECT THIS PIN TO GROUND.
 2. GROUND PADDLE. CONNECT THE GROUND PADDLE TO A GROUND PLANE THAT HAS LOW ELECTRICAL AND THERMAL IMPEDANCE.

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Input. The RFIN pin is DC-coupled and matched to 50 Ω. See Figure 3 for the interface schematic.
2, 6	GND	Ground. Connect to a ground plane that has low electrical and thermal impedance. See Figure 4 for the interface schematic.
3	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDDx to set I _{DQ} . See Figure 121 and Table 8 for more details. See Figure 5 for the interface schematic.
4, 7	NIC	No Internal Connection. The NIC pin is not connected internally. For normal operation, connect the NIC pin to ground.
5	RFOUT/VDD1	RF Output and Drain Bias Voltage. The RF output is DC-coupled and also serves as the drain biasing node. For the drain bias voltage, connect a DC bias network to provide the drain current and AC-couple the RF output path. See Figure 6 for the interface schematic.
8	ACG/VDD2	AC Ground and Optional Alternative Drain Bias. Connect a capacitor between the ACG/VDD2 pin and ground. The ACG/VDD2 pin can also be used as the drain biasing node through an internal resistor. Do not use the ACG/VDD2 pin simultaneously with the RFOUT/VDD1 pin. See Figure 6 for the interface schematic.
	GROUND PADDLE	Ground Paddle. Connect the ground paddle to a ground plane that has low electrical and thermal impedance.

INTERFACE SCHEMATICS

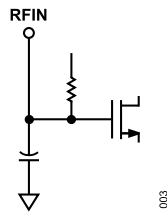


Figure 3. RFIN Interface Schematic

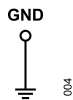


Figure 4. GND Interface Schematic

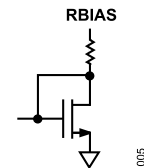


Figure 5. RBIAS Interface Schematic

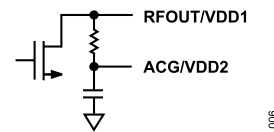


Figure 6. RFOUT/VDD1 and ACG/VDD2 Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

10 MHz TO 22 GHz BIAS TEE

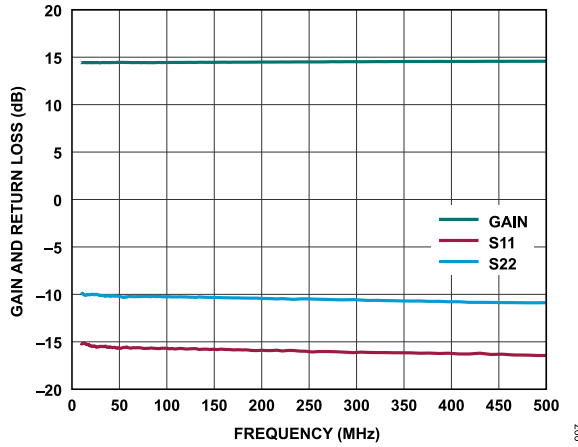


Figure 7. Gain and Return Loss vs. Frequency, 10 MHz to 500 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

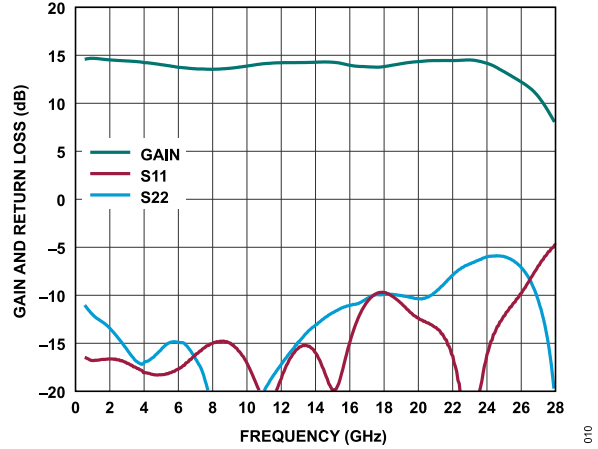


Figure 10. Gain and Return Loss vs. Frequency, 500 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

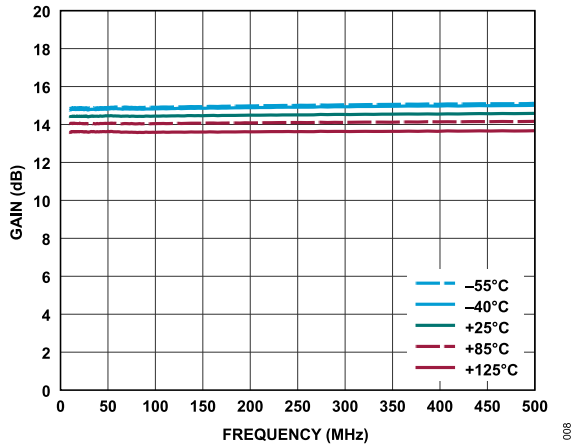


Figure 8. Gain vs. Frequency for Various Temperatures, 10 MHz to 500 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

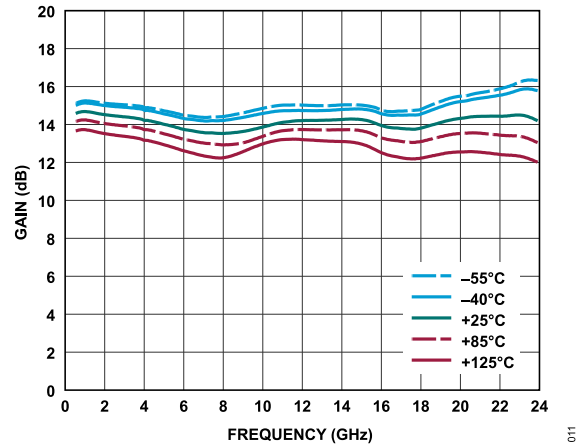


Figure 11. Gain vs. Frequency for Various Temperatures, 500 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

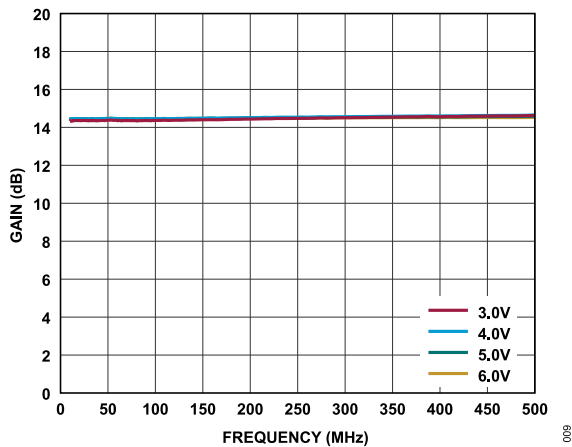


Figure 9. Gain vs. Frequency for Various Supply Voltages, 10 MHz to 500 MHz and $I_{DQ} = 90\text{ mA}$

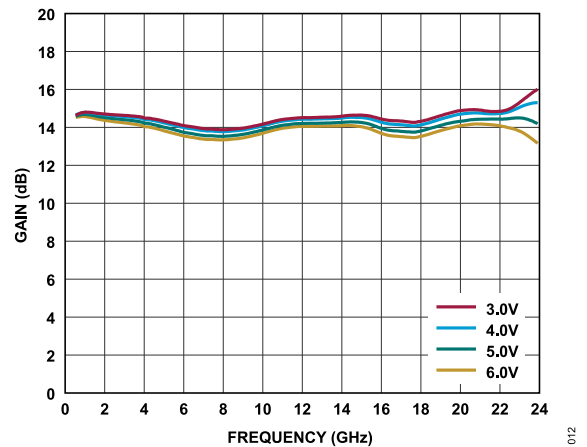


Figure 12. Gain vs. Frequency for Various Supply Voltages, 500 MHz to 24 GHz, and $I_{DQ} = 90\text{ mA}$

TYPICAL PERFORMANCE CHARACTERISTICS

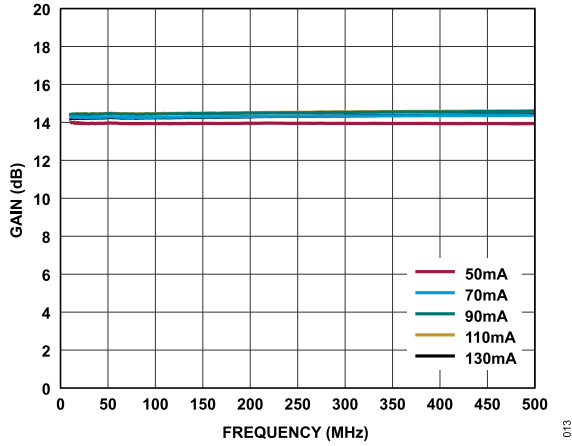


Figure 13. Gain vs. Frequency for Various I_{DQ} Values, 10 MHz to 500 MHz, and $V_{DD} = 5 V$

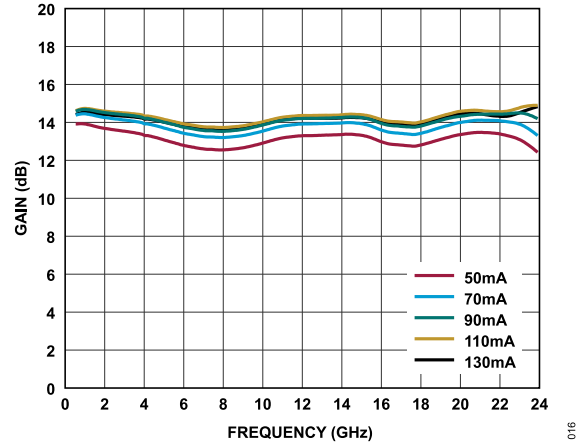


Figure 16. Gain vs. Frequency for Various I_{DQ} Values, 500 MHz to 24 GHz, and $V_{DD} = 5 V$

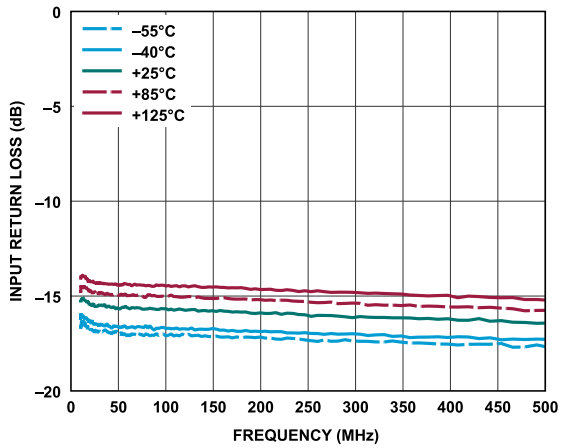


Figure 14. Input Return Loss vs. Frequency for Various Temperatures, 10 MHz to 500 MHz, $V_{DD} = 5 V$, $I_{DQ} = 90 mA$, and $R_{BIAS} = 715 \Omega$

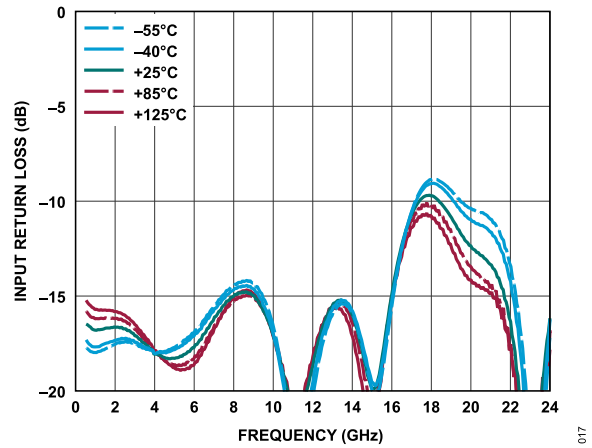


Figure 17. Input Return Loss vs. Frequency for Various Temperatures, 500 MHz to 24 GHz, $V_{DD} = 5 V$, $I_{DQ} = 90 mA$, and $R_{BIAS} = 715 \Omega$

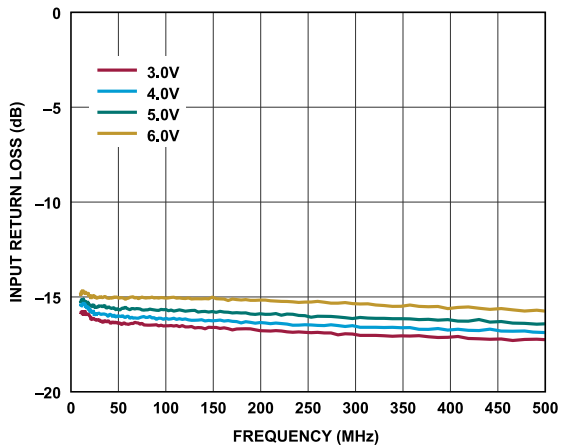


Figure 15. Input Return Loss vs. Frequency for Various Supply Voltages, 10 MHz to 500 MHz, and $I_{DQ} = 90 mA$

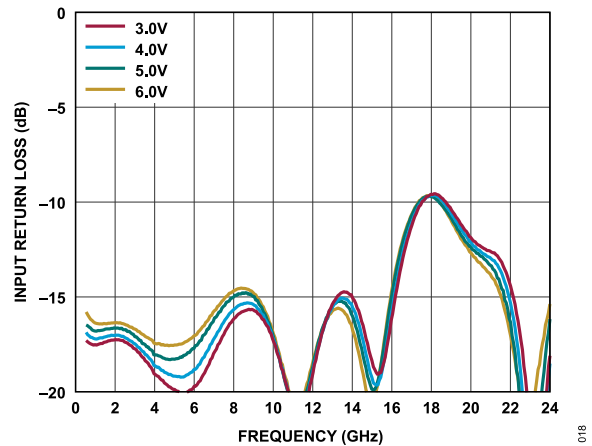


Figure 18. Input Return Loss vs. Frequency for Various Supply Voltages, 500 MHz to 24 GHz, and $I_{DQ} = 90 mA$

TYPICAL PERFORMANCE CHARACTERISTICS

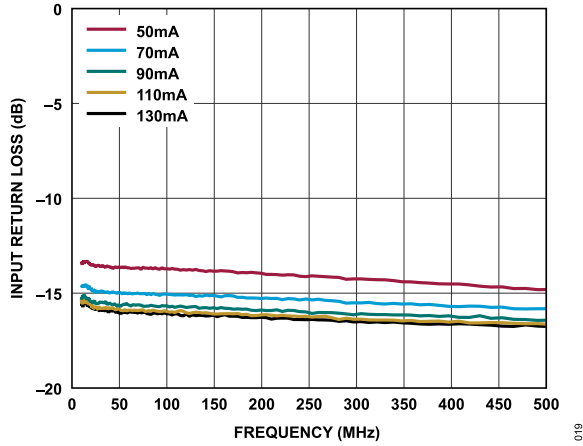


Figure 19. Input Return Loss vs. Frequency for Various I_{DQ} Values, 10 MHz to 500 MHz, and $V_{DD} = 5 V$

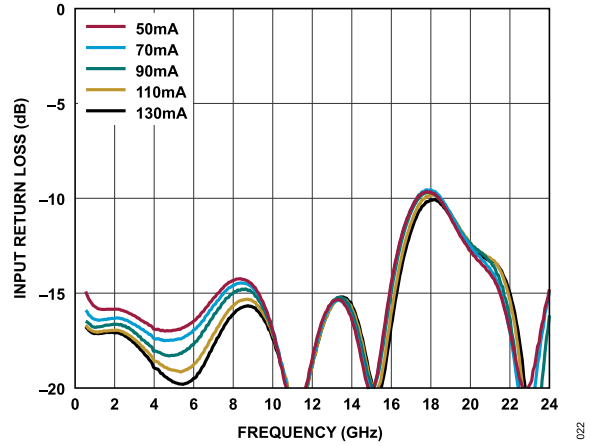


Figure 22. Input Return Loss vs. Frequency for Various I_{DQ} Values, 500 MHz to 24 GHz, and $V_{DD} = 5 V$

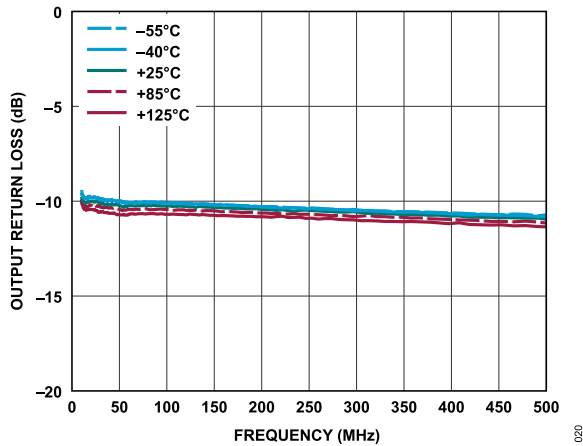


Figure 20. Output Return Loss vs. Frequency for Various Temperatures, 10 MHz to 500 MHz, $V_{DD} = 5 V$, $I_{DQ} = 90 mA$, and $R_{BIAS} = 715 \Omega$

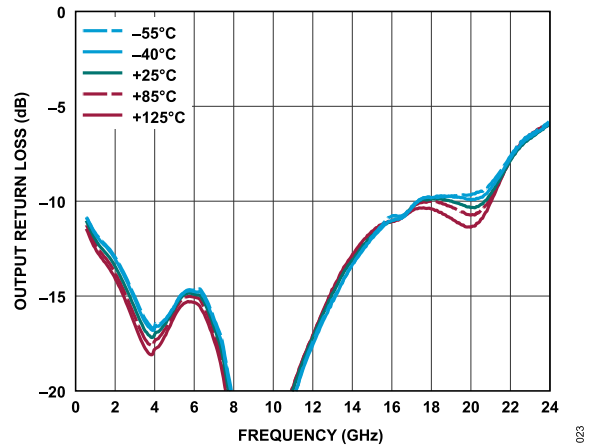


Figure 23. Output Return Loss vs. Frequency for Various Temperatures, 500 MHz to 24 GHz, $V_{DD} = 5 V$, $I_{DQ} = 90 mA$, and $R_{BIAS} = 715 \Omega$

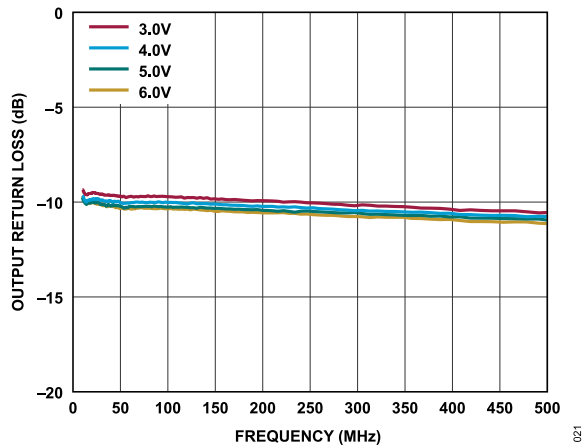


Figure 21. Output Return Loss vs. Frequency for Various Supply Voltages, 10 MHz to 500 MHz, and $I_{DQ} = 90 mA$

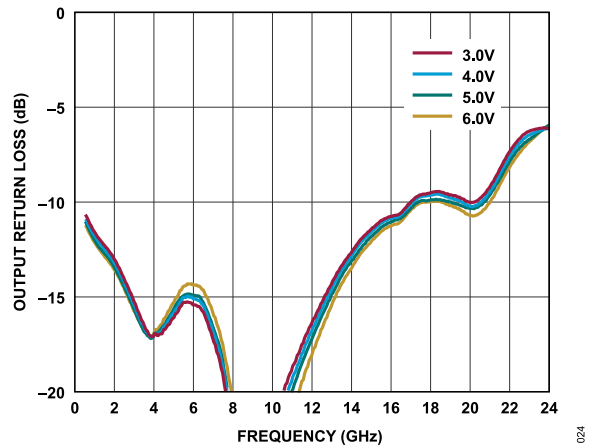


Figure 24. Output Return Loss vs. Frequency for Various Supply Voltages, 500 MHz to 24 GHz, and $I_{DQ} = 90 mA$

TYPICAL PERFORMANCE CHARACTERISTICS

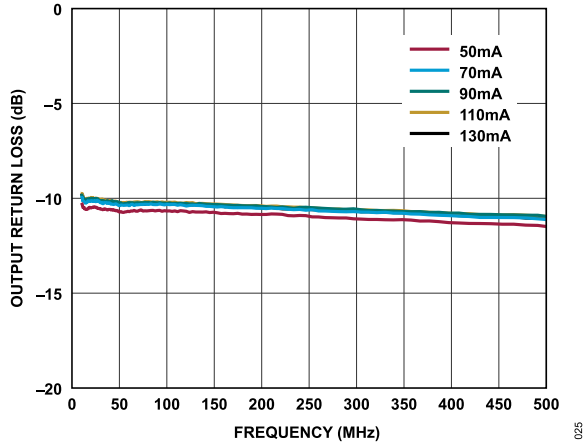


Figure 25. Output Return Loss vs. Frequency for Various I_{DQ} Values, 10 MHz to 500 MHz, and $V_{DD} = 5 V$

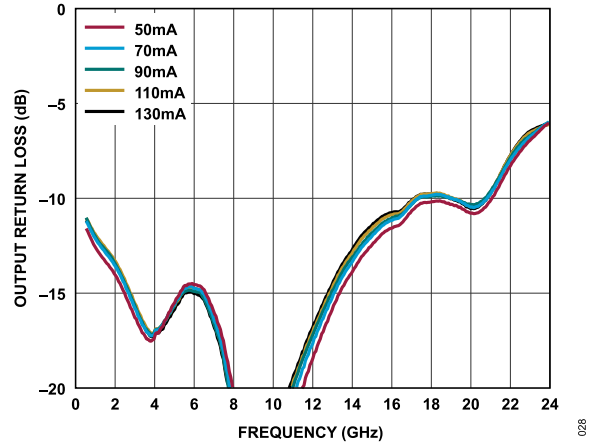


Figure 28. Output Return Loss vs. Frequency for Various I_{DQ} Values, 500 MHz to 24 GHz, and $V_{DD} = 5 V$

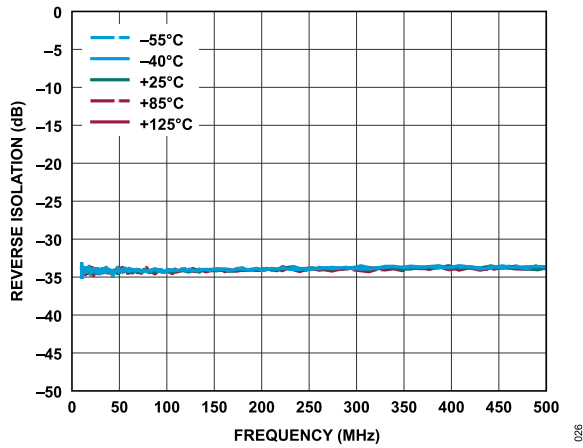


Figure 26. Reverse Isolation vs. Frequency for Various Temperatures, 10 MHz to 500 MHz, $V_{DD} = 5 V$, $I_{DQ} = 90 mA$, and $R_{BIAS} = 715 \Omega$

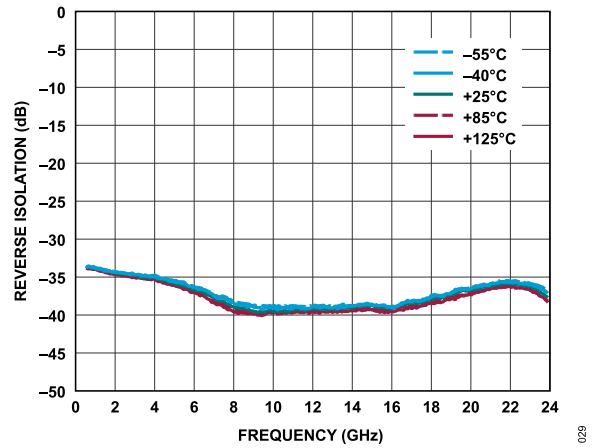


Figure 29. Reverse Isolation vs. Frequency for Various Temperatures, 500 MHz to 24 GHz, $V_{DD} = 5 V$, $I_{DQ} = 90 mA$, and $R_{BIAS} = 715 \Omega$

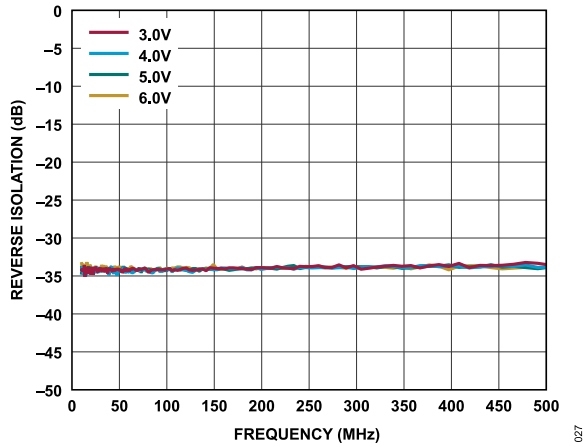


Figure 27. Reverse Isolation vs. Frequency for Various Supply Voltages, 10 MHz to 500 MHz, and $I_{DQ} = 90 mA$

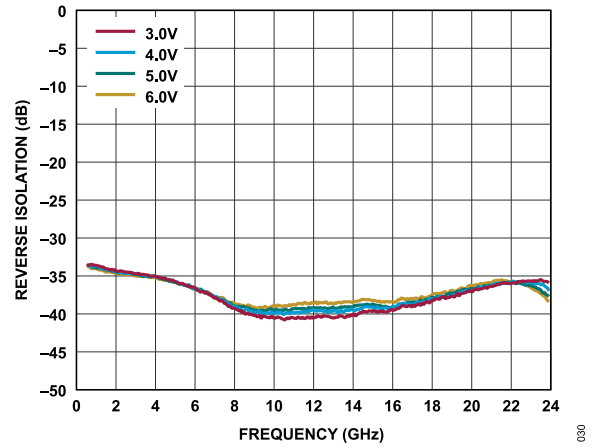


Figure 30. Reverse Isolation vs. Frequency for Various Supply Voltages, 500 MHz to 24 GHz, and $I_{DQ} = 90 mA$

TYPICAL PERFORMANCE CHARACTERISTICS

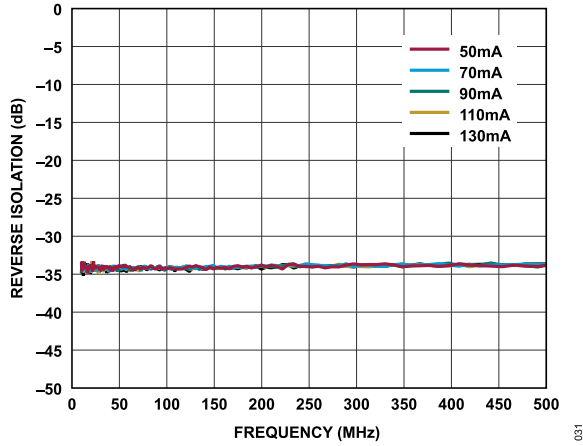


Figure 31. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 10 MHz to 500 MHz, and $V_{DD} = 5 V$

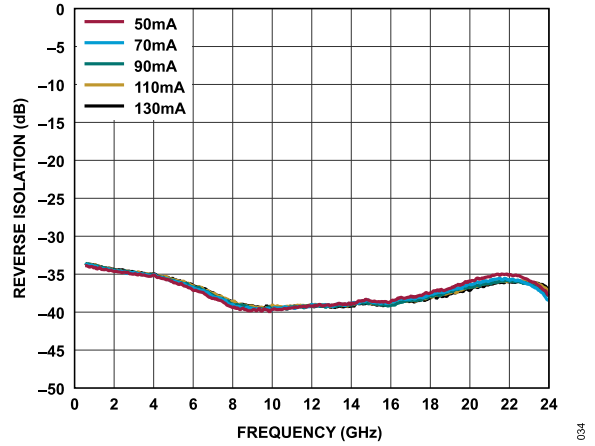


Figure 34. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 500 MHz to 24 GHz, and $V_{DD} = 5 V$

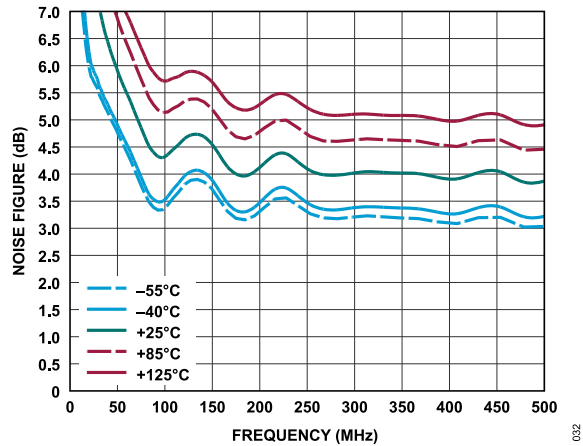


Figure 32. Noise Figure vs. Frequency for Various Temperatures, 10 MHz to 500 MHz, $V_{DD} = 5 V$, $I_{DQ} = 90 mA$, and $R_{BIAS} = 715 \Omega$

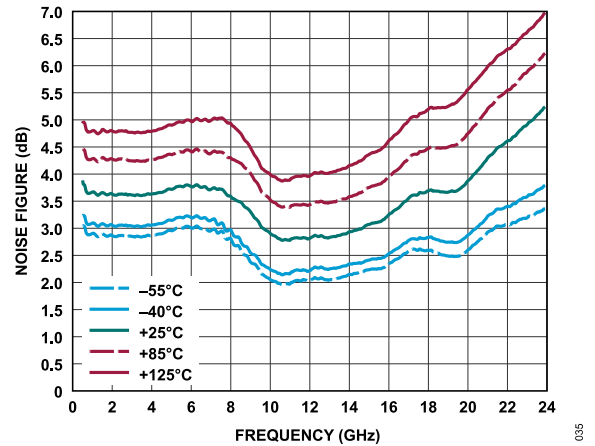


Figure 35. Noise Figure vs. Frequency for Various Temperatures, 500 MHz to 24 GHz, $V_{DD} = 5 V$, $I_{DQ} = 90 mA$, and $R_{BIAS} = 715 \Omega$

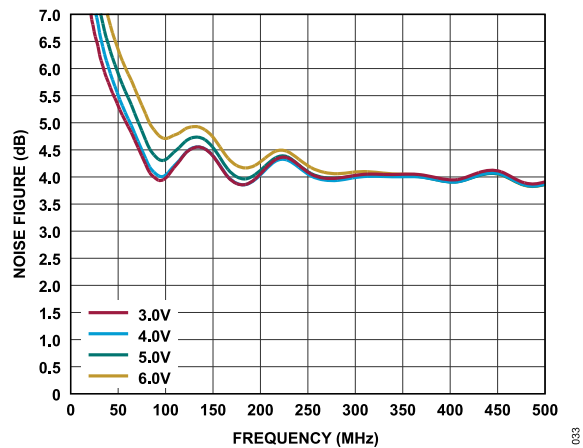


Figure 33. Noise Figure vs. Frequency for Various Supply Voltages, 10 MHz to 500 MHz, and $I_{DQ} = 90 mA$

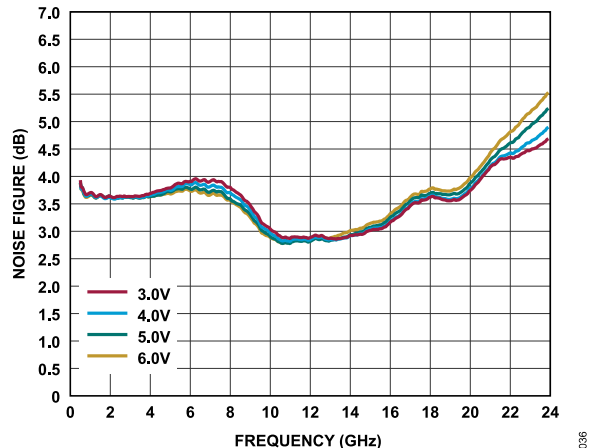


Figure 36. Noise Figure vs. Frequency for Various Supply Voltages, 500 MHz to 24 GHz, and $I_{DQ} = 90 mA$

TYPICAL PERFORMANCE CHARACTERISTICS

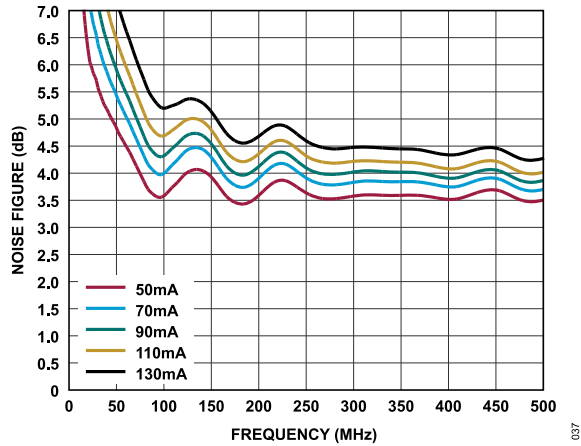


Figure 37. Noise Figure vs. Frequency for Various I_{DQ} Values, 10 MHz to 500 MHz, and $V_{DD} = 5\text{ V}$

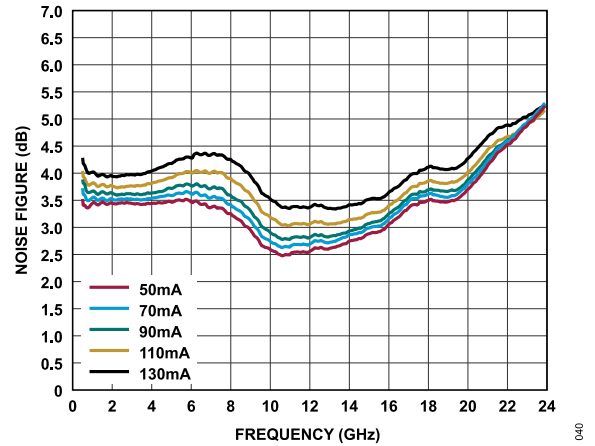


Figure 40. Noise Figure vs. Frequency for Various I_{DQ} Values, 500 MHz to 24 GHz, and $V_{DD} = 5\text{ V}$

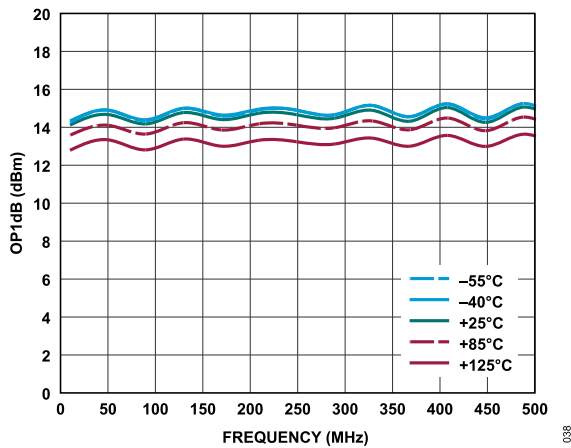


Figure 38. OP1dB vs. Frequency for Various Temperatures, 10 MHz to 500 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

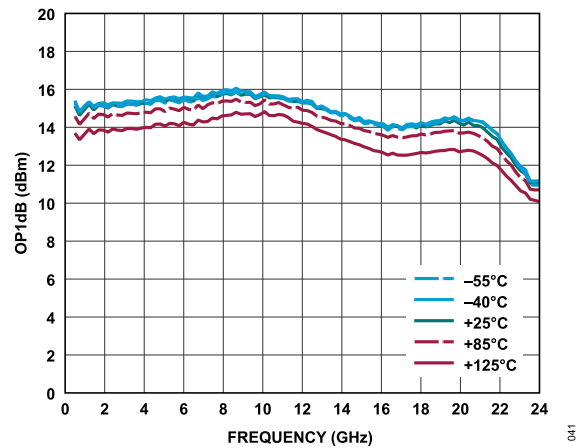


Figure 41. OP1dB vs. Frequency for Various Temperatures, 500 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

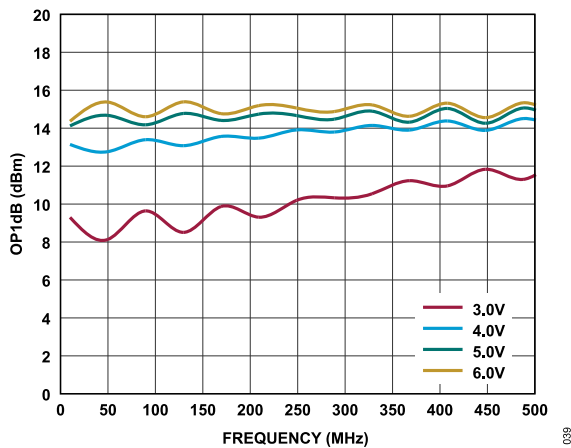


Figure 39. OP1dB vs. Frequency for Various Supply Voltages, 10 MHz to 500 MHz, and $I_{DQ} = 90\text{ mA}$

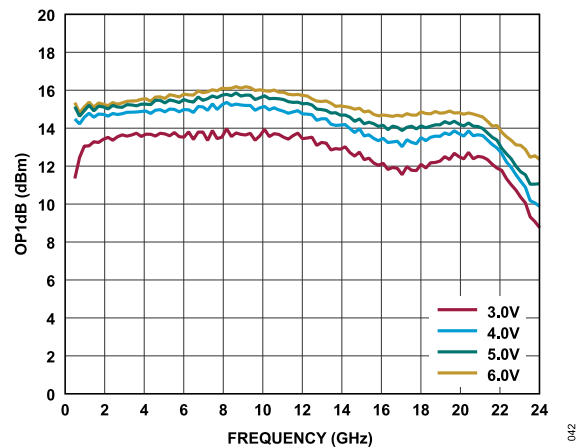


Figure 42. OP1dB vs. Frequency for Various Supply Voltages, 500 MHz to 24 GHz, and $I_{DQ} = 90\text{ mA}$

TYPICAL PERFORMANCE CHARACTERISTICS

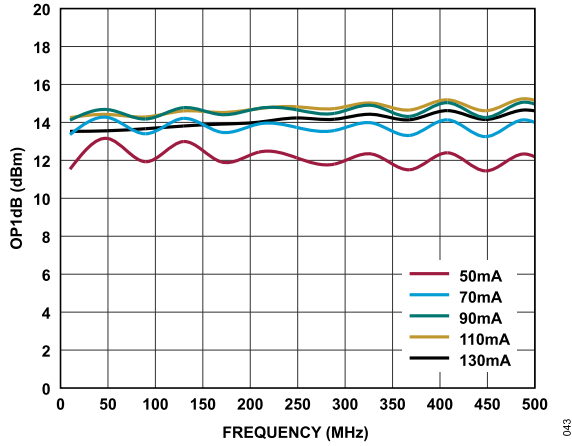


Figure 43. OP1dB vs. Frequency for Various I_{DQ} Values, 10 MHz to 500 MHz, and $V_{DD} = 5\text{ V}$

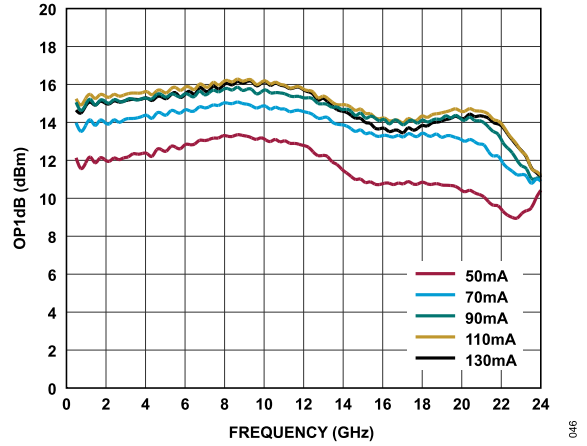


Figure 46. OP1dB vs. Frequency for Various I_{DQ} Values, 500 MHz to 24 GHz, and $V_{DD} = 5\text{ V}$

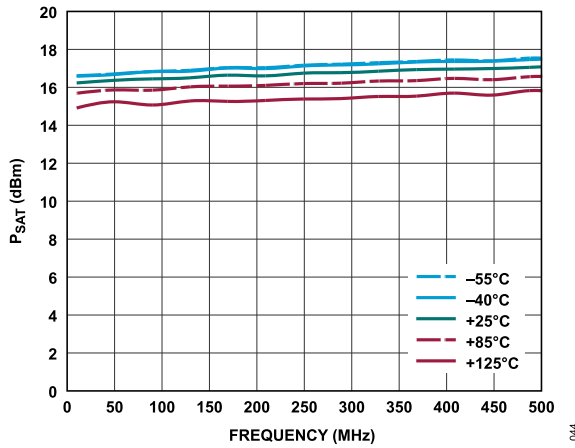


Figure 44. P_{SAT} vs. Frequency for Various Temperatures, 10 MHz to 500 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

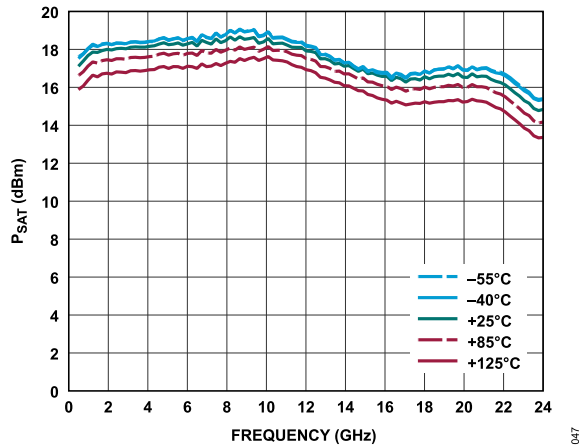


Figure 47. P_{SAT} vs. Frequency for Various Temperatures, 500 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

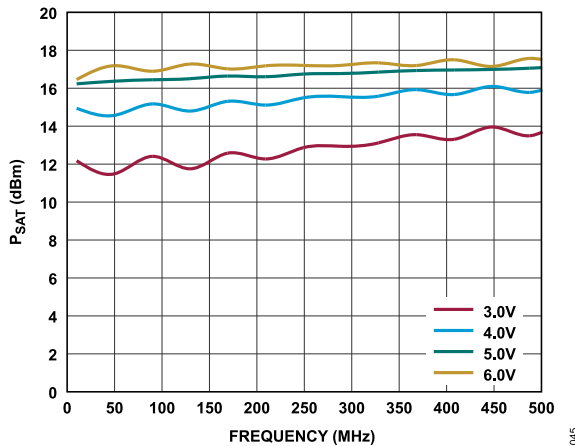


Figure 45. P_{SAT} vs. Frequency for Various Supply Voltages, 10 MHz to 500 MHz, and $I_{DQ} = 90\text{ mA}$

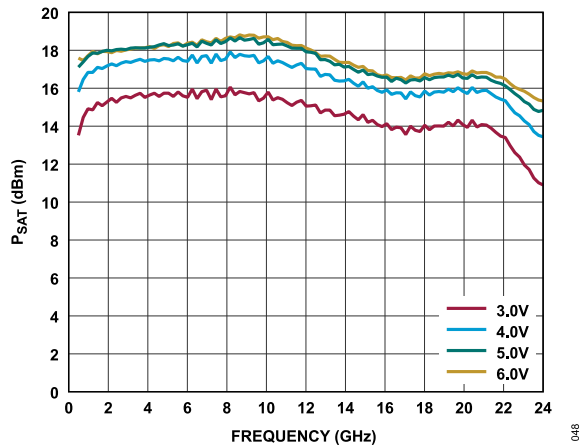


Figure 48. P_{SAT} vs. Frequency for Various Supply Voltages, 500 MHz to 24 GHz, and $I_{DQ} = 90\text{ mA}$

TYPICAL PERFORMANCE CHARACTERISTICS

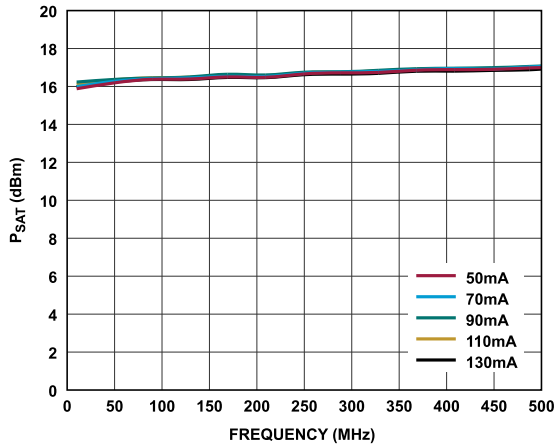


Figure 49. P_{SAT} vs. Frequency for Various I_{DQ} Values, 10 MHz to 500 MHz, and $I_{DQ} = 90$ mA

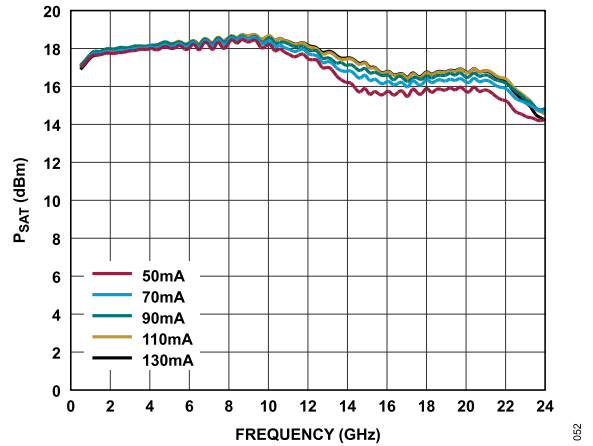


Figure 52. P_{SAT} vs. Frequency for Various I_{DQ} Values, 500 MHz to 24 GHz, and $I_{DQ} = 90$ mA

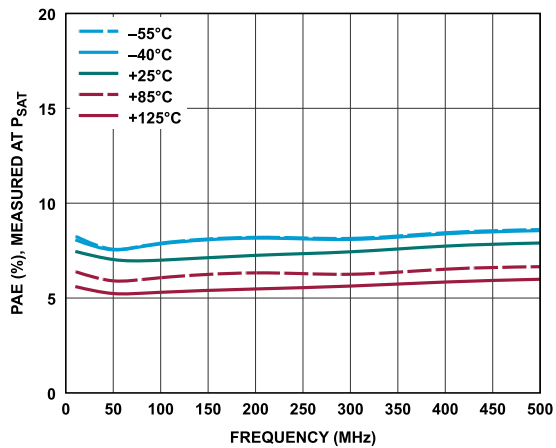


Figure 50. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 10 MHz to 500 MHz, $V_{DD} = 5$ V, $I_{DQ} = 90$ mA, and $R_{BIAS} = 715 \Omega$

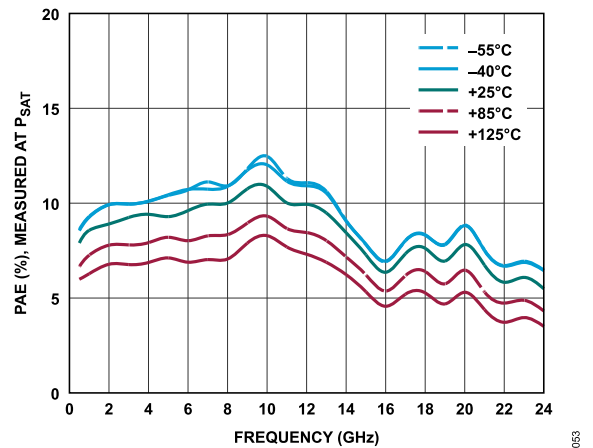


Figure 53. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 500 MHz to 24 GHz, $V_{DD} = 5$ V, $I_{DQ} = 90$ mA, and $R_{BIAS} = 715 \Omega$

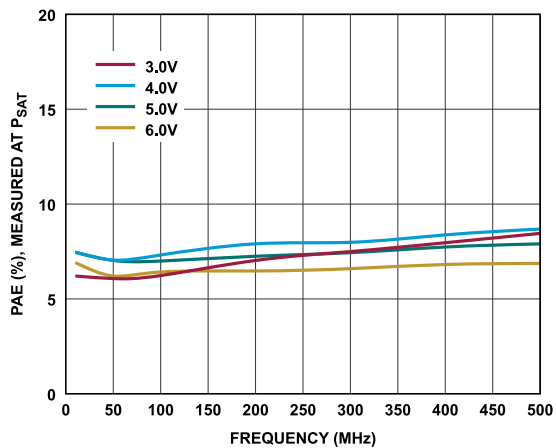


Figure 51. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 10 MHz to 500 MHz, and $I_{DQ} = 90$ mA

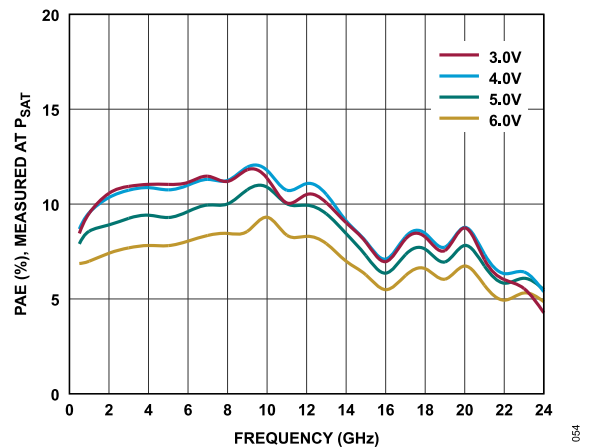


Figure 54. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 500 MHz to 24 GHz, and $I_{DQ} = 90$ mA

TYPICAL PERFORMANCE CHARACTERISTICS

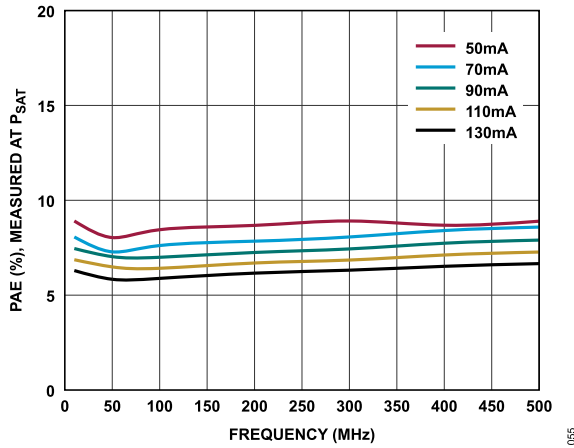


Figure 55. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 10 MHz to 500 MHz, and $I_{DQ} = 90$ mA

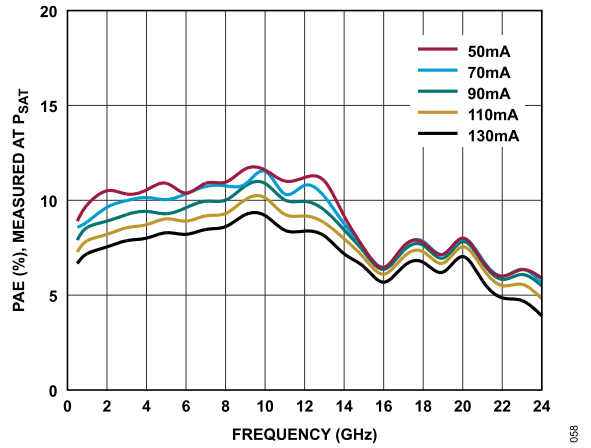


Figure 58. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 500 MHz to 24 GHz, and $I_{DQ} = 90$ mA

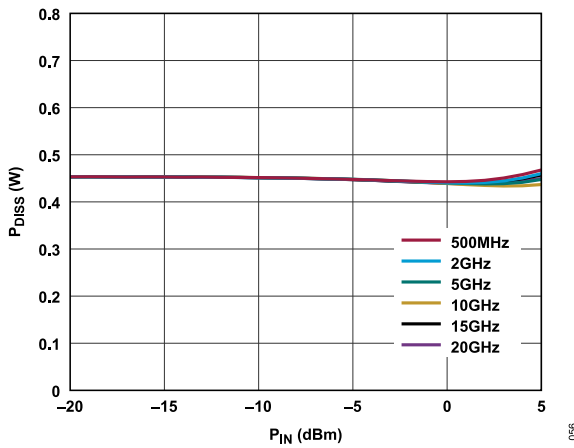


Figure 56. P_{DISS} vs. P_{IN} at Various Frequencies, $T_{CASE} = 85^{\circ}C$, and $V_{DD} = 5$ V

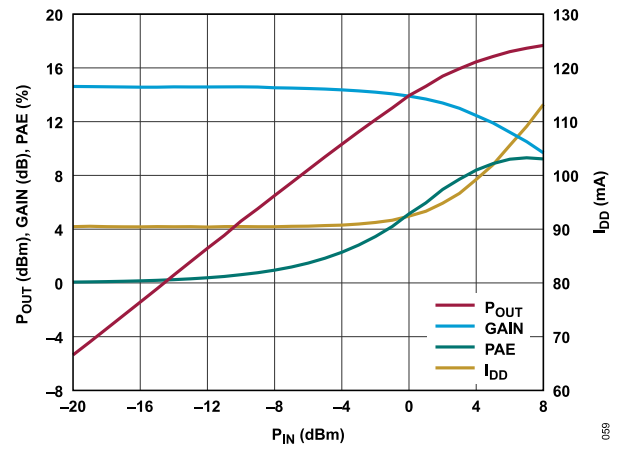


Figure 59. P_{OUT} , GAIN, PAE, and I_{DD} vs. P_{IN} , Power Compression at 2 GHz, $V_{DD} = 5$ V, and $R_{BIAS} = 715 \Omega$

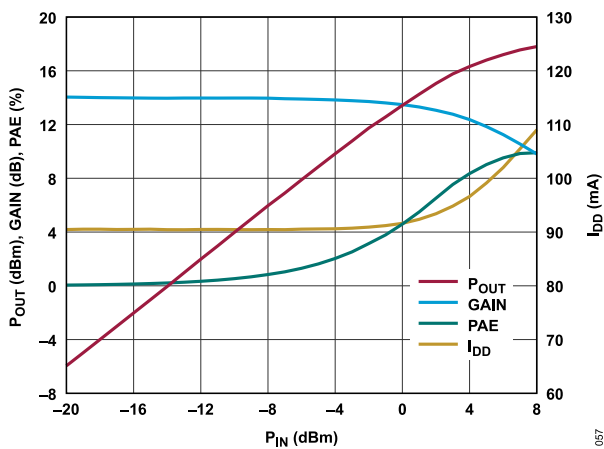


Figure 57. P_{OUT} , GAIN, PAE, and I_{DD} vs. P_{IN} , Power Compression at 10 GHz, $V_{DD} = 5$ V, and $R_{BIAS} = 715 \Omega$

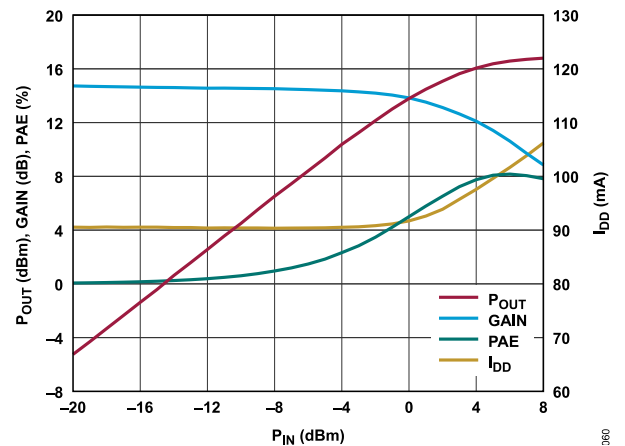


Figure 60. P_{OUT} , GAIN, PAE, and I_{DD} vs. P_{IN} , Power Compression at 20 GHz, $V_{DD} = 5$ V, and $R_{BIAS} = 715 \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

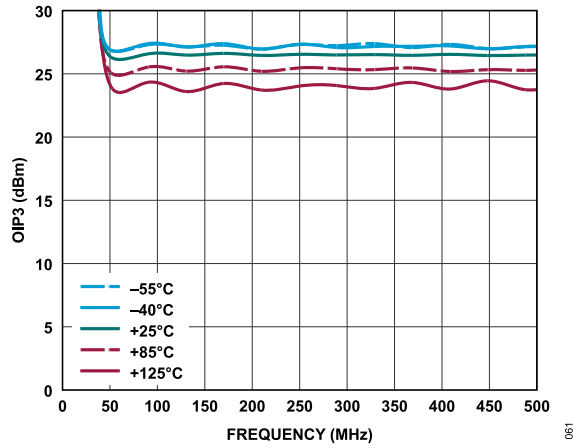


Figure 61. OIP3 vs. Frequency for Various Temperatures, 10 MHz to 500 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

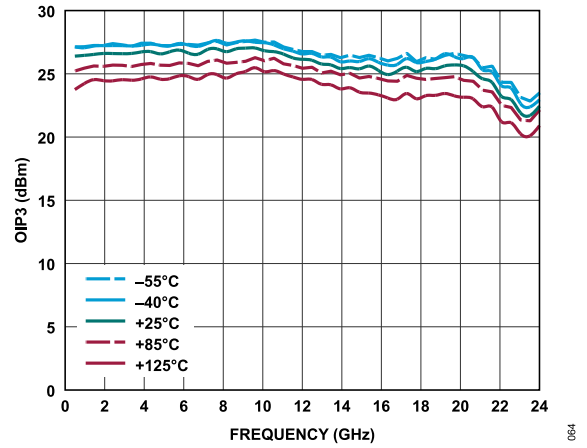


Figure 64. OIP3 vs. Frequency for Various Temperatures, 500 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

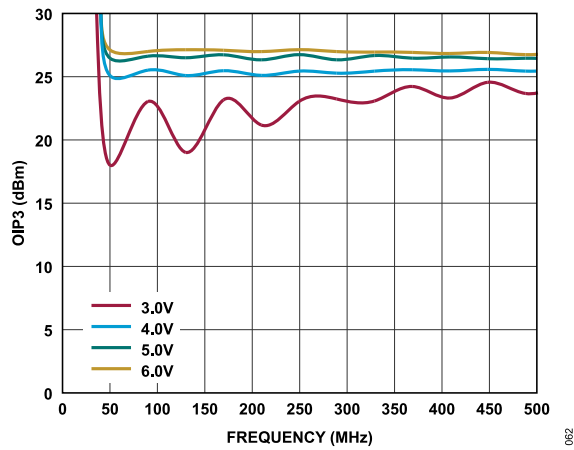


Figure 62. OIP3 vs. Frequency for Various Supply Voltages, 10 MHz to 500 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

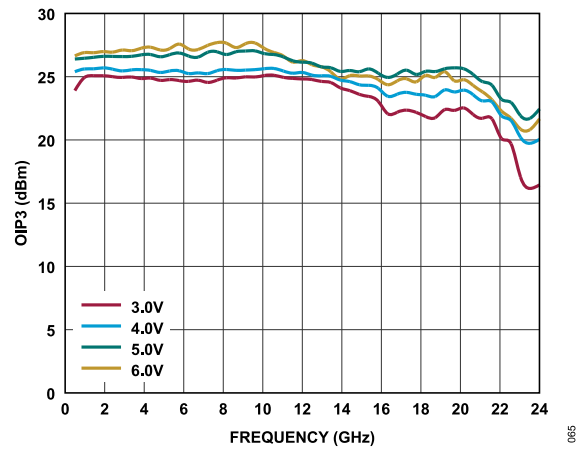


Figure 65. OIP3 vs. Frequency for Various Supply Voltages, 500 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

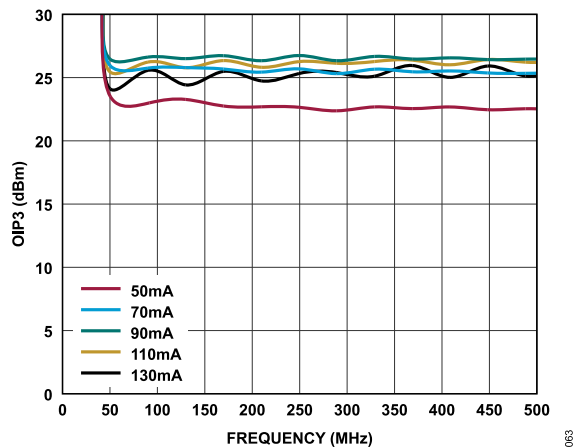


Figure 63. OIP3 vs. Frequency for Various I_{DQ} Values, 10 MHz to 500 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

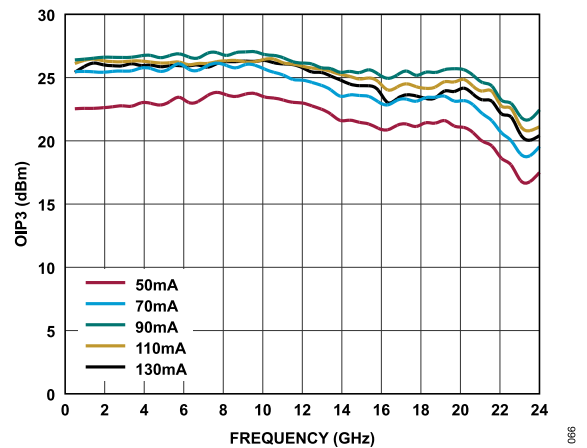


Figure 66. OIP3 vs. Frequency for Various I_{DQ} Values, 500 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

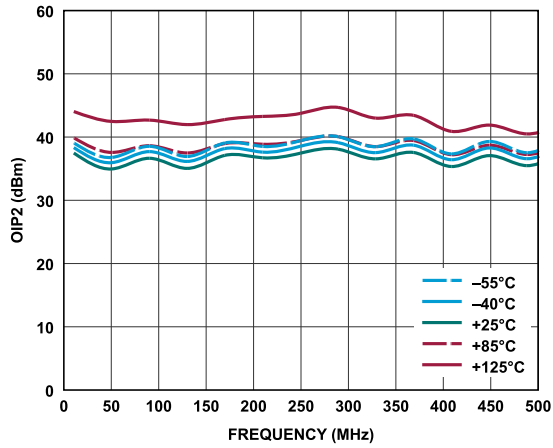


Figure 67. OIP2 vs. Frequency for Various Temperatures, 10 MHz to 500 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

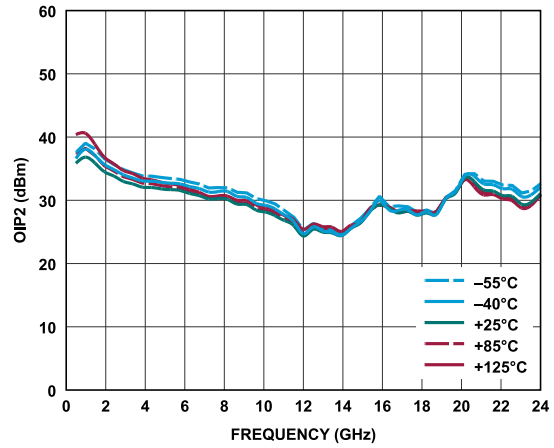


Figure 70. OIP2 vs. Frequency for Various Temperatures, 500 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

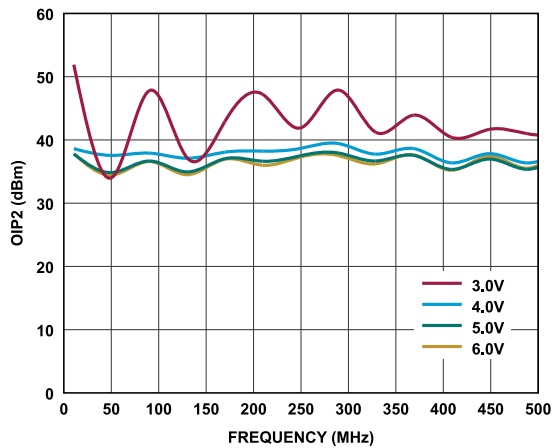


Figure 68. OIP2 vs. Frequency for Various Supply Voltages, 10 MHz to 500 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

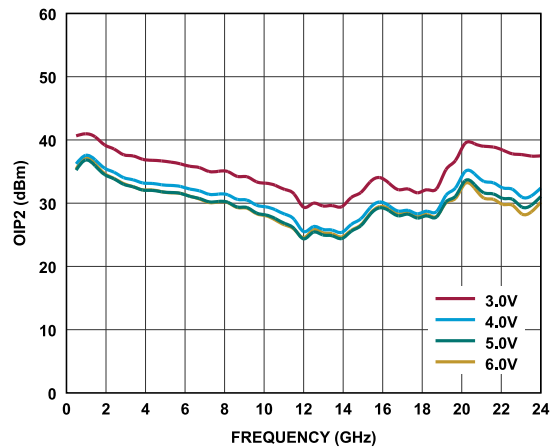


Figure 71. OIP2 vs. Frequency for Various Supply Voltages, 500 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

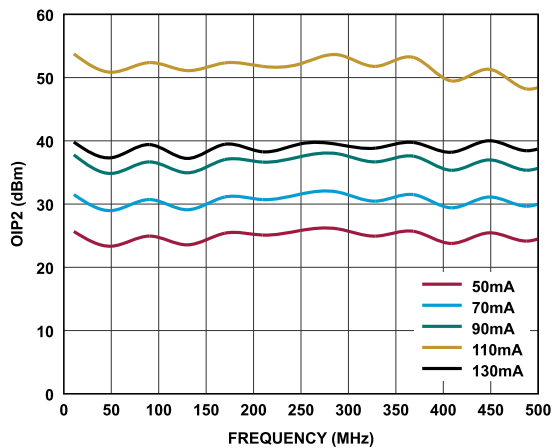


Figure 69. OIP2 vs. Frequency for I_{DQ} Values, 10 MHz to 500 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

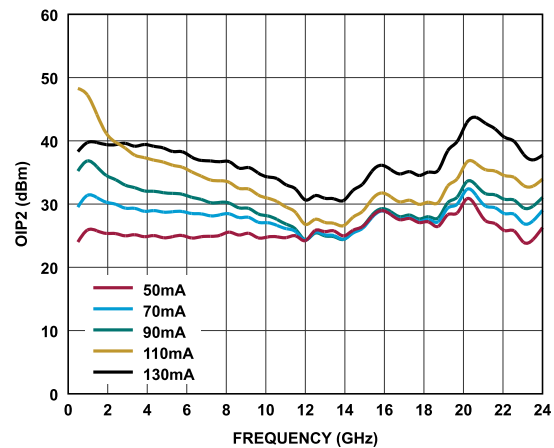


Figure 72. OIP2 vs. Frequency for I_{DQ} Values, 500 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

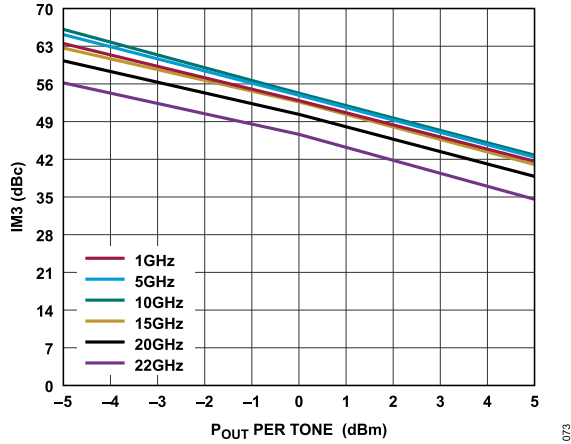


Figure 73. Third-Order Intermodulation Distortion (IM3) vs. P_{OUT} per Tone for Various Frequencies, $V_{DD} = 5\text{ V}$, and $R_{BIAS} = 715\ \Omega$

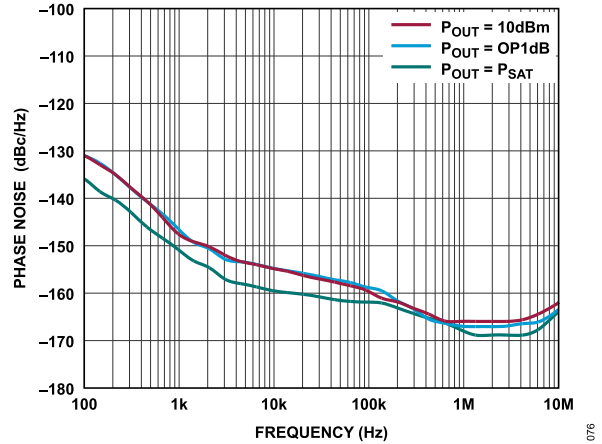


Figure 76. Phase Noise vs. Frequency at 2 GHz for Various P_{OUT} Values

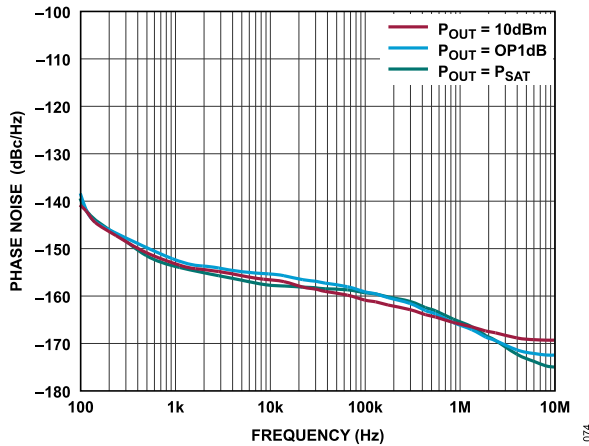


Figure 74. Phase Noise vs. Frequency at 5 GHz for Various P_{OUT} Values

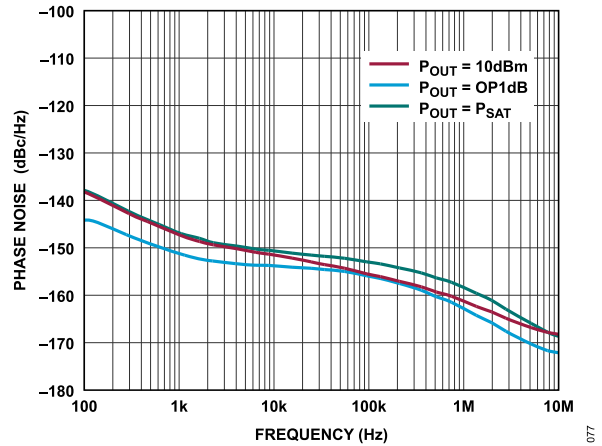


Figure 77. Phase Noise vs. Frequency at 10 GHz for Various P_{OUT} Values

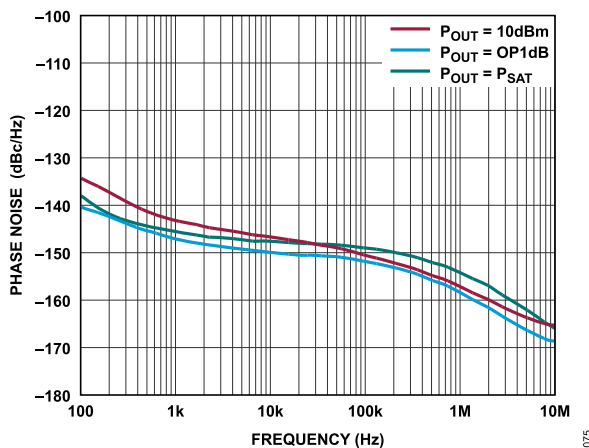


Figure 75. Phase Noise vs. Frequency at 15 GHz for Various P_{OUT} Values

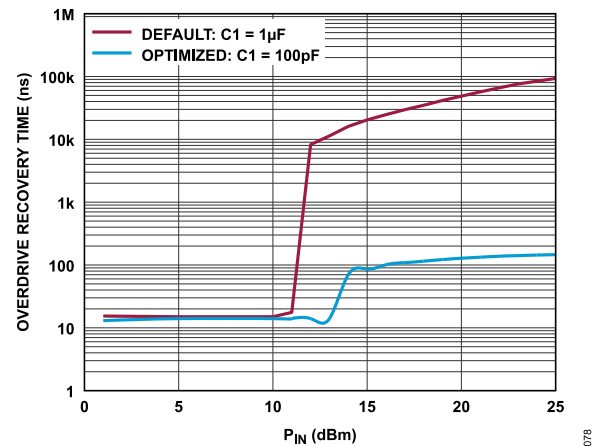


Figure 78. Overdrive Recovery Time vs. P_{IN} at 6 GHz, Recovery Time to Within 90% of Small Signal Gain Value, $V_{DD} = 5\text{ V}$, and $R_{BIAS} = 715\ \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

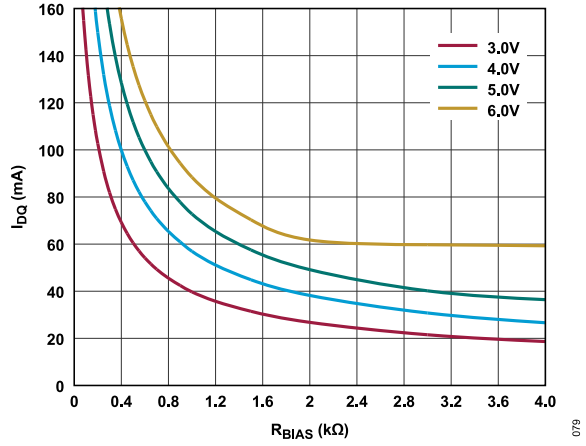


Figure 79. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 0 Ω to 4 k Ω

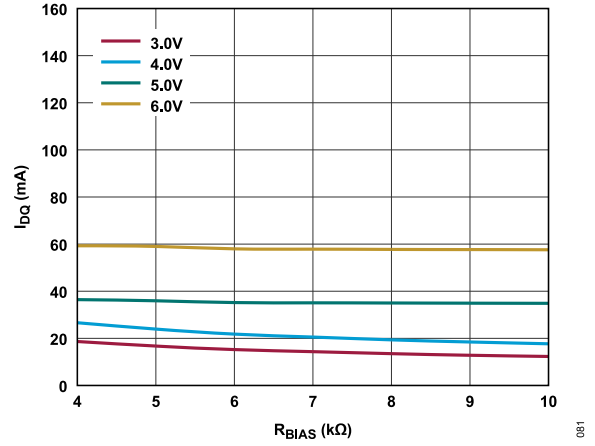


Figure 81. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 4 k Ω to 10 k Ω

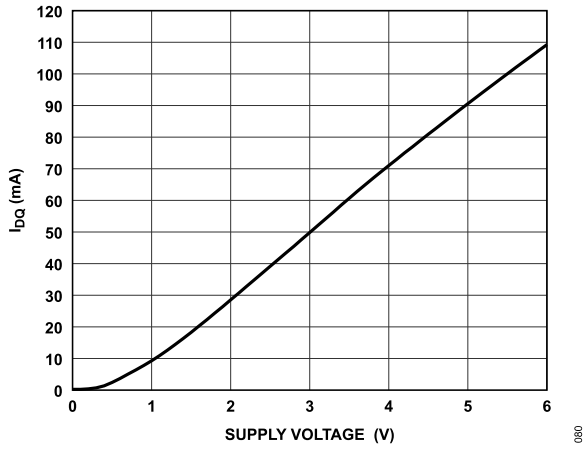


Figure 80. I_{DQ} vs. Supply Voltage, $R_{BIAS} = 715 \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

10 MHZ TO 22 GHZ BIAS TEE, BIASING THROUGH THE ACG/VDD2 PIN

$V_{DD2} = 8.5\text{ V}$, $V_{BIAS} = 5\text{ V}$, and frequency range = 0.01 GHz to 24 GHz.

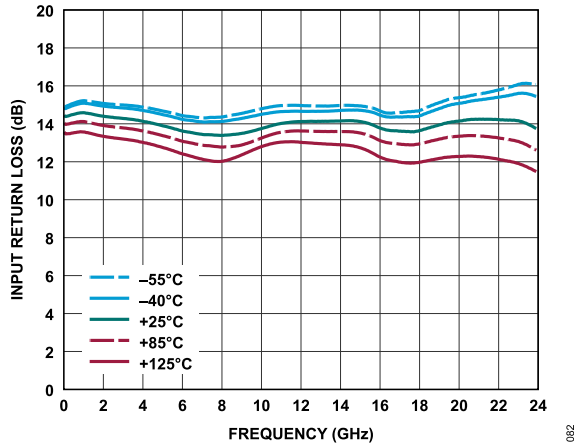


Figure 82. Gain vs. Frequency for Various Temperatures, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

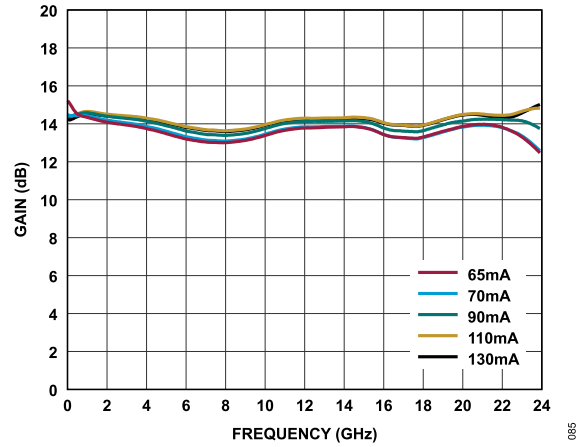


Figure 85. Gain vs. Frequency for Various I_{DQ} Values

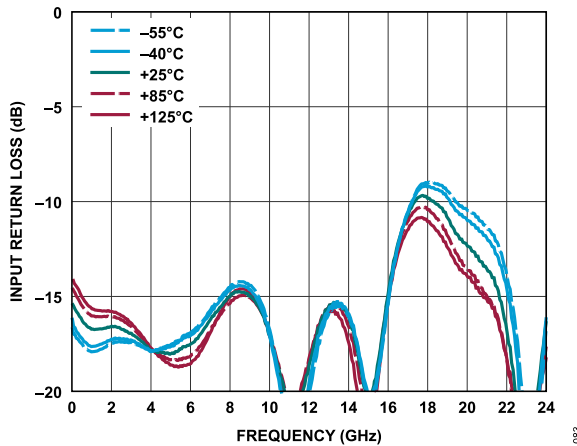


Figure 83. Input Return Loss vs. Frequency for Various Temperatures, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

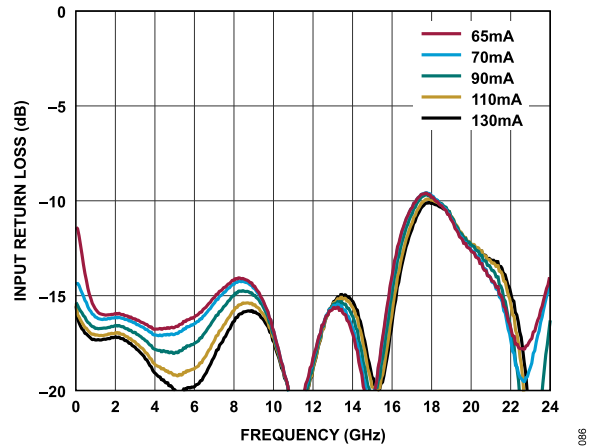


Figure 86. Input Return Loss vs. Frequency for Various I_{DQ} Values

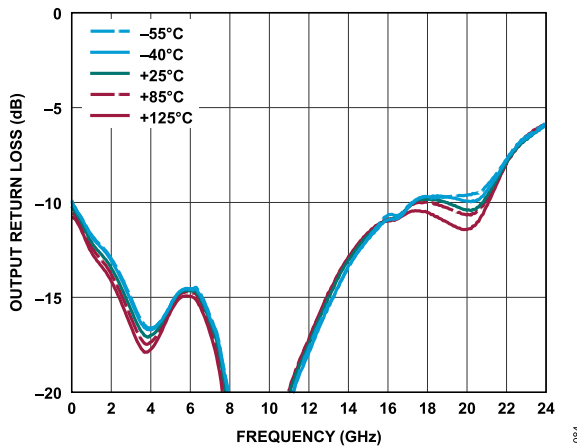


Figure 84. Output Return Loss vs. Frequency for Various Temperatures, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

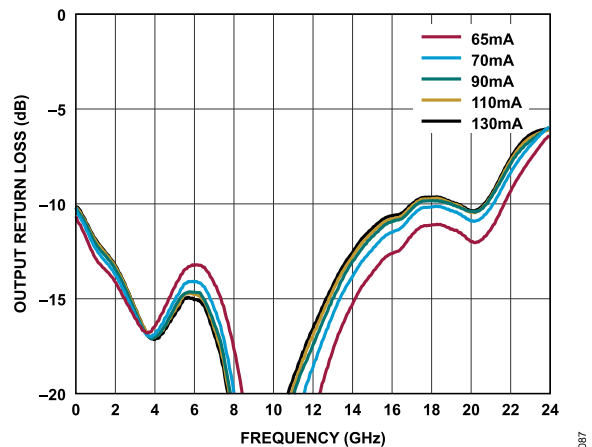


Figure 87. Output Return Loss vs. Frequency for Various I_{DQ} Values

TYPICAL PERFORMANCE CHARACTERISTICS

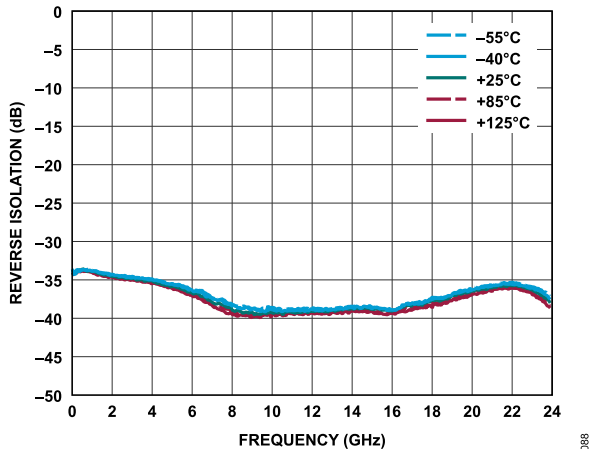


Figure 88. Reverse Isolation vs. Frequency for Various Temperatures, $I_{DQ} = 90 \text{ mA}$, and $R_{BIAS} = 715 \Omega$

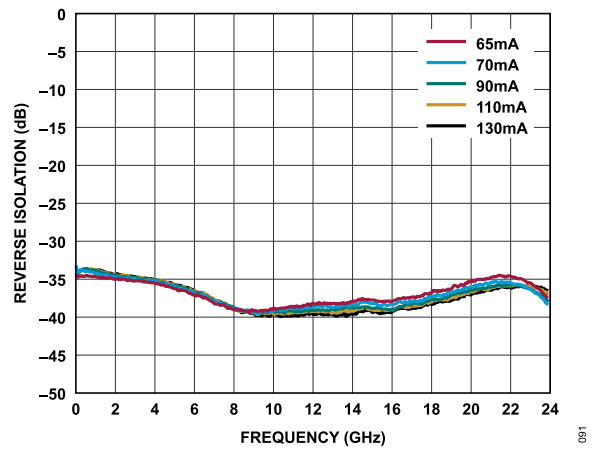


Figure 91. Reverse Isolation vs. Frequency for Various I_{DQ} Values

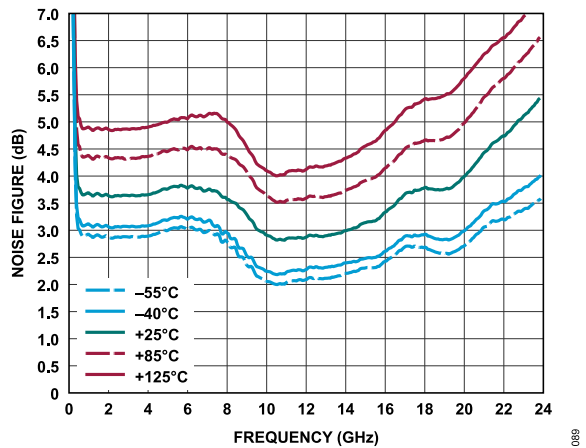


Figure 89. Noise Figure vs. Frequency for Various Temperatures, $I_{DQ} = 90 \text{ mA}$, and $R_{BIAS} = 715 \Omega$

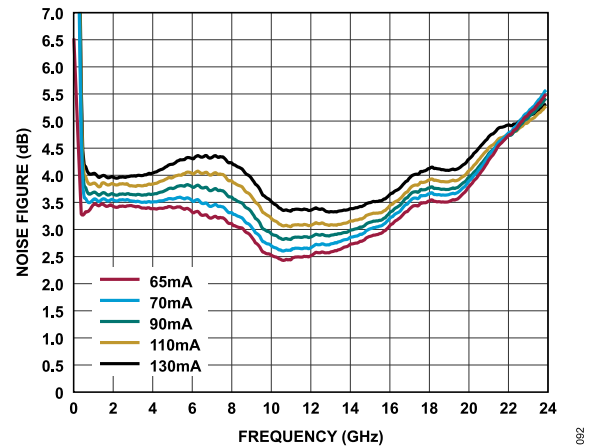


Figure 92. Noise Figure vs. Frequency for Various I_{DQ} Values

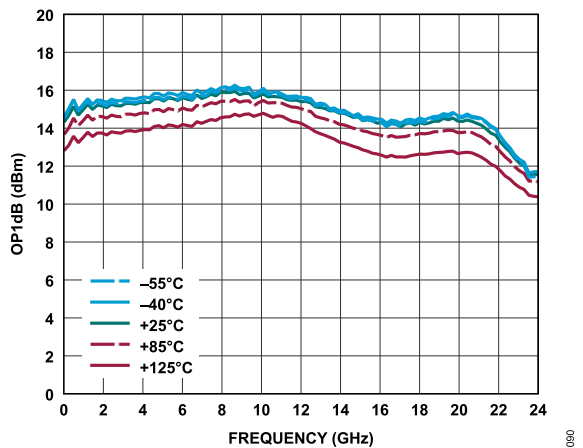


Figure 90. OP1dB vs. Frequency for Various Temperatures, $I_{DQ} = 90 \text{ mA}$, and $R_{BIAS} = 715 \Omega$

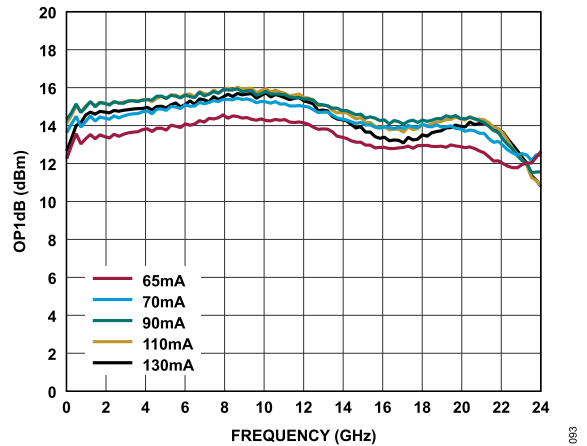


Figure 93. OP1dB vs. Frequency for Various I_{DQ} Values

TYPICAL PERFORMANCE CHARACTERISTICS

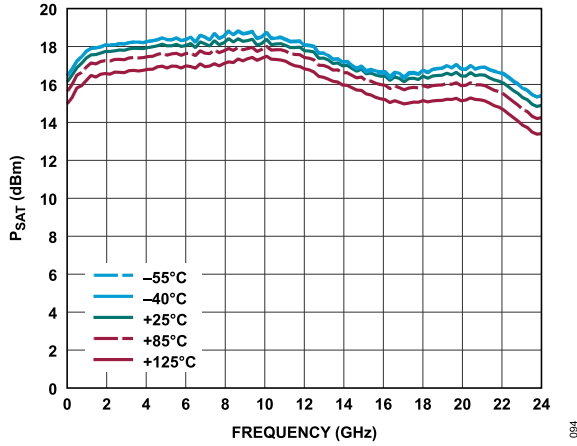


Figure 94. P_{SAT} vs. Frequency for Various Temperatures, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

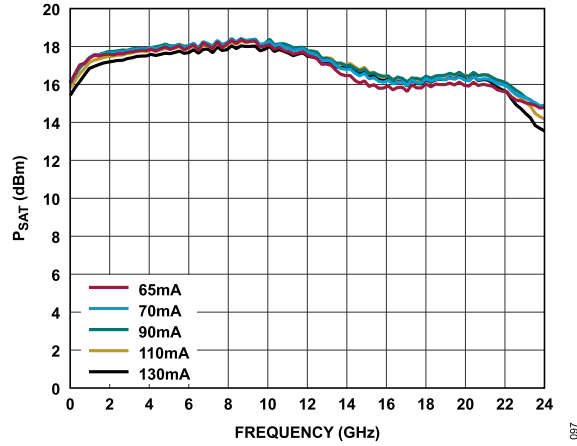


Figure 97. P_{SAT} vs. Frequency for Various I_{DQ} Values

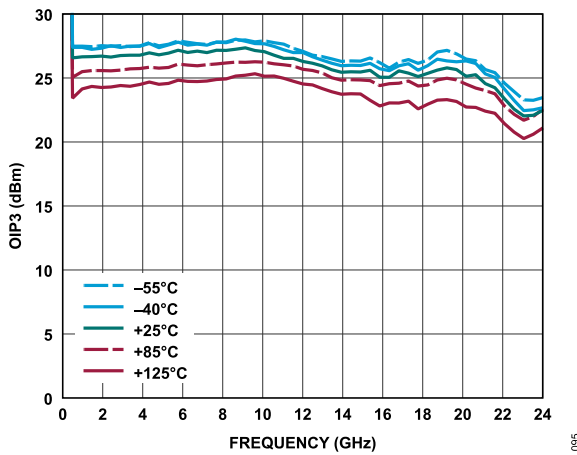


Figure 95. $OIP3$ vs. Frequency for Various Temperatures, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

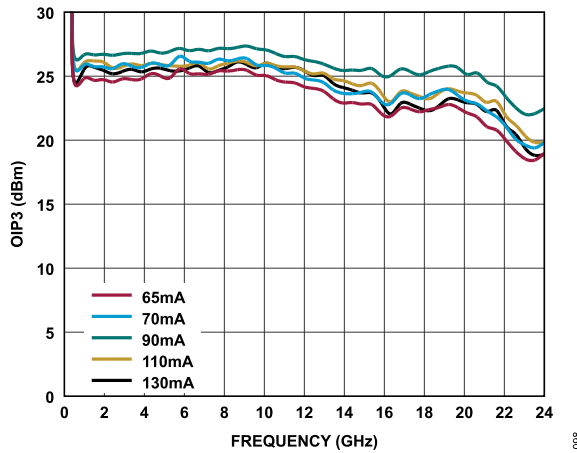


Figure 98. $OIP3$ vs. Frequency for Various I_{DQ} Values

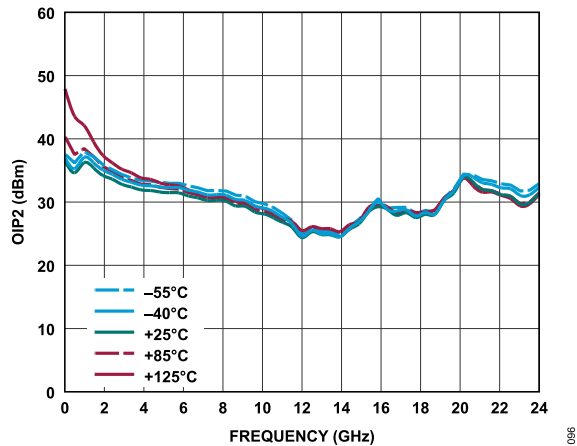


Figure 96. $OIP2$ vs. Frequency for Various Temperatures, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

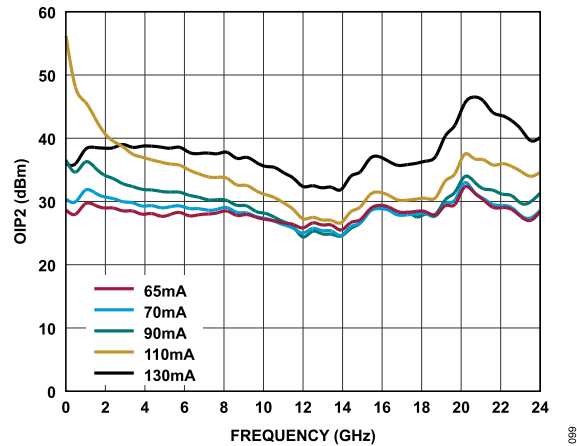


Figure 99. $OIP2$ vs. Frequency for Various I_{DQ} Values

TYPICAL PERFORMANCE CHARACTERISTICS

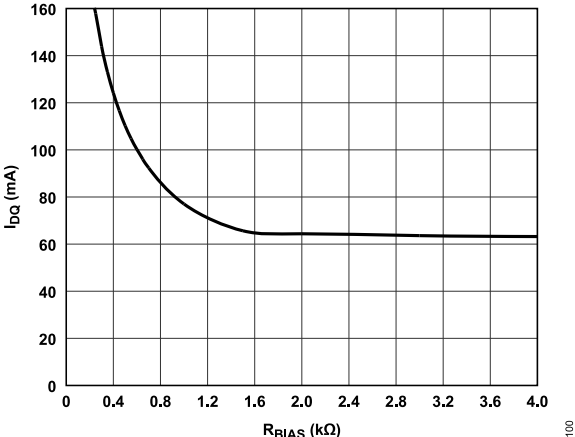


Figure 100. I_{DQ} vs. R_{BIAS}, 0 Ω to 4 kΩ

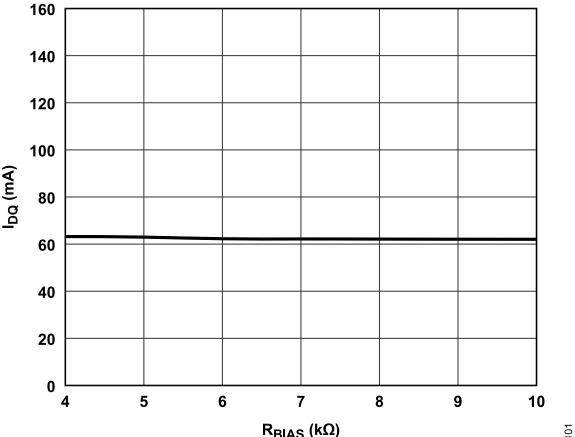


Figure 101. I_{DQ} vs. R_{BIAS}, 4 kΩ to 10 kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

10 KHZ TO 22 GHZ BIAS TEE

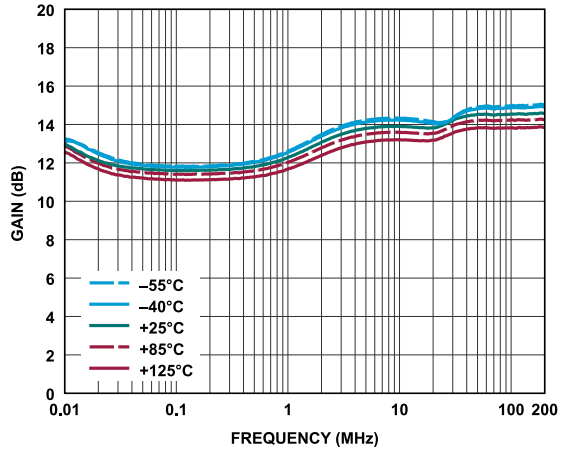


Figure 102. Gain vs. Frequency for Various Temperatures, 10 kHz to 200 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

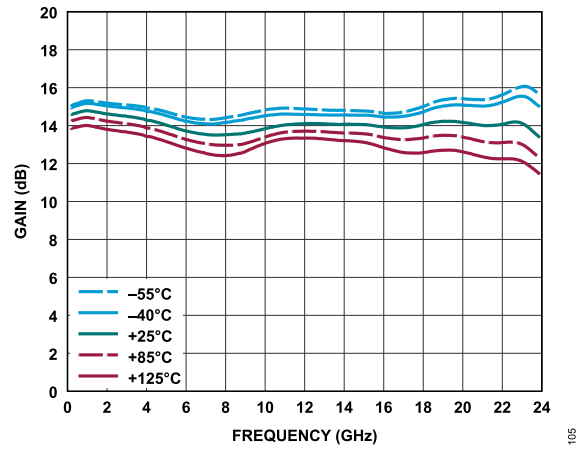


Figure 105. Gain vs. Frequency for Various Temperatures, 200 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

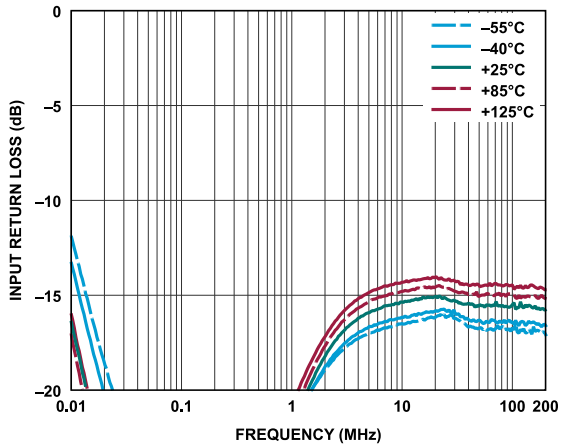


Figure 103. Input Return Loss vs. Frequency for Various Temperatures, 10 kHz to 200 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

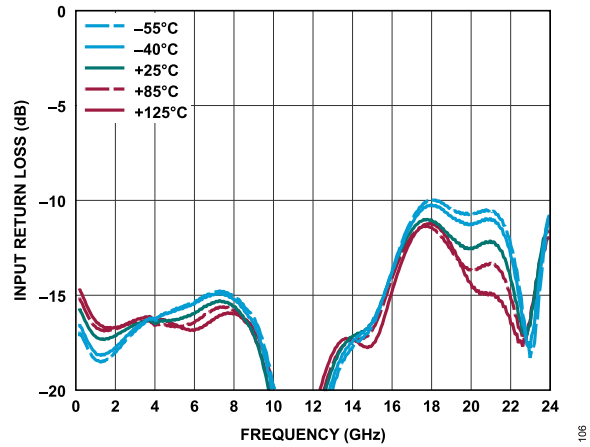


Figure 106. Input Return Loss vs. Frequency for Various Temperatures, 200 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

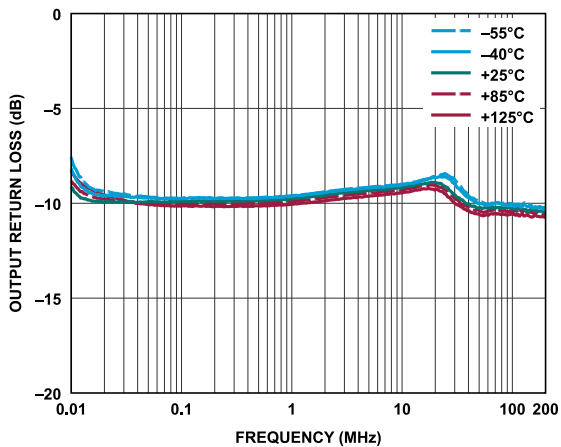


Figure 104. Output Return Loss vs. Frequency for Various Temperatures, 10 kHz to 200 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

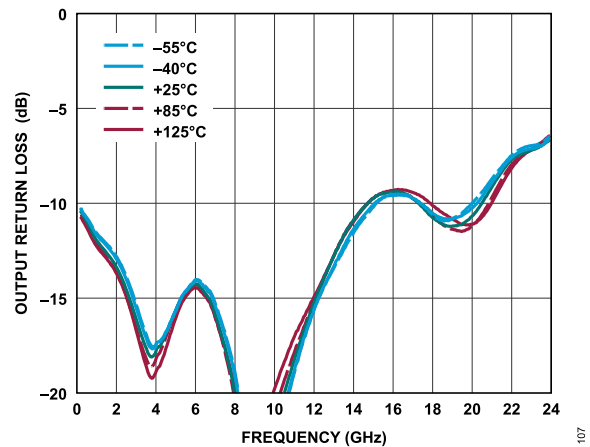


Figure 107. Output Return Loss vs. Frequency for Various Temperatures, 200 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

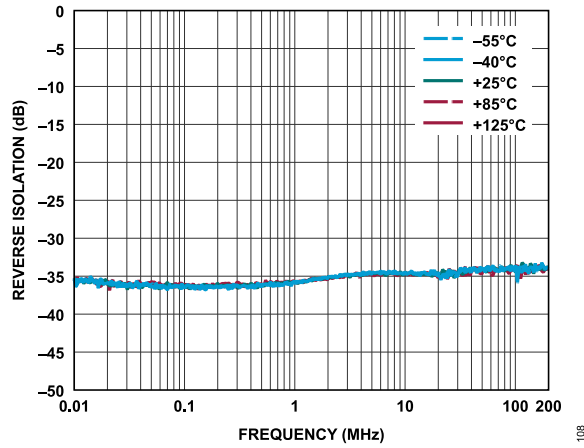


Figure 108. Reverse Isolation vs. Frequency for Various Temperatures, 10 kHz to 200 MHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

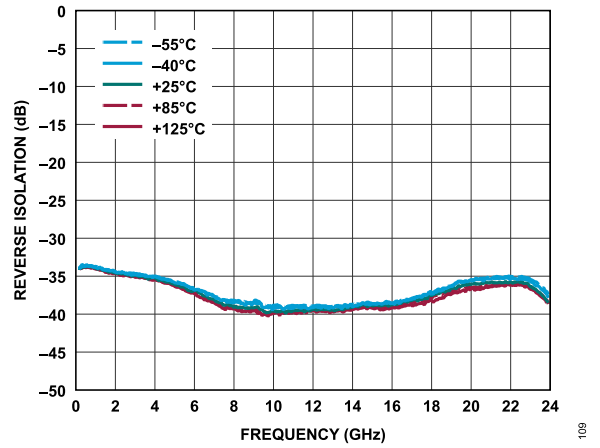


Figure 109. Reverse Isolation vs. Frequency for Various Temperatures, 200 MHz to 24 GHz, $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, and $R_{BIAS} = 715\ \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

10 KHZ TO 22 GHZ BIAS TEE, BIASING THROUGH THE ACG/VDD2 PIN

$V_{DD2} = 8.5\text{ V}$, $V_{BIAS} = 5\text{ V}$, and $R_{BIAS} = 715\ \Omega$.

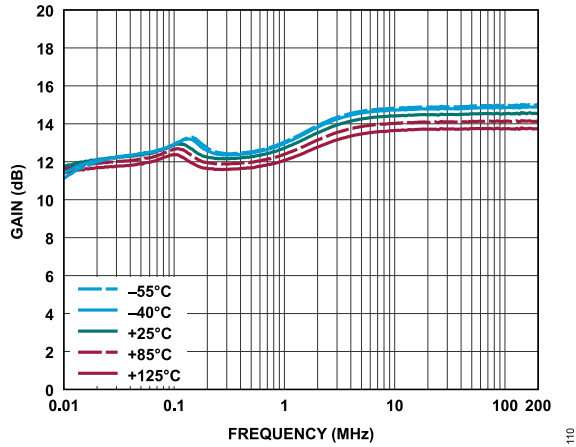


Figure 110. Gain vs. Frequency for Various Temperatures, 10 kHz to 200 MHz

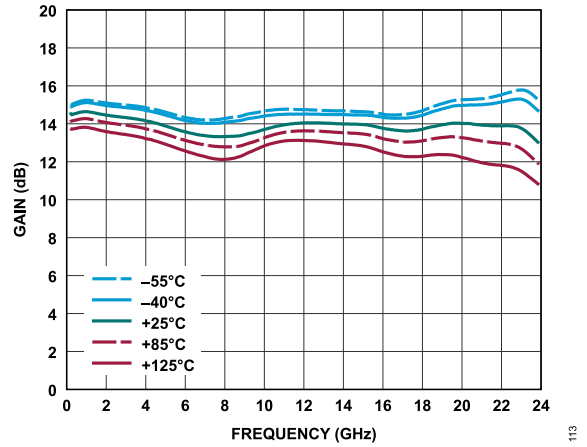


Figure 113. Gain vs. Frequency for Various Temperatures, 200 MHz to 24 GHz

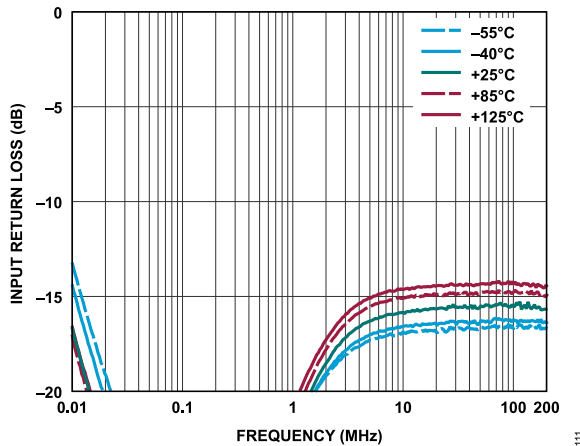


Figure 111. Input Return Loss vs. Frequency for Various Temperatures, 10 kHz to 200 MHz

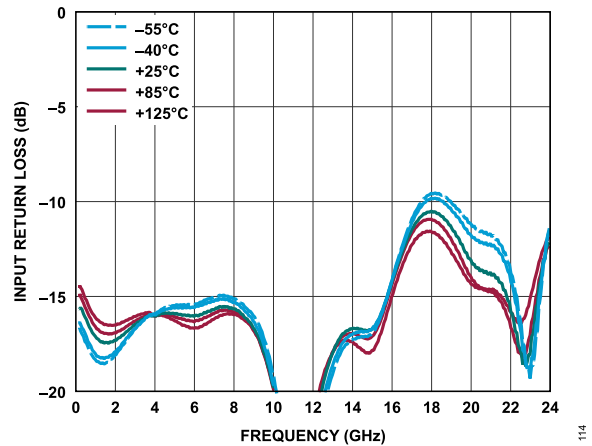


Figure 114. Input Return Loss vs. Frequency for Various Temperatures, 200 MHz to 24 GHz

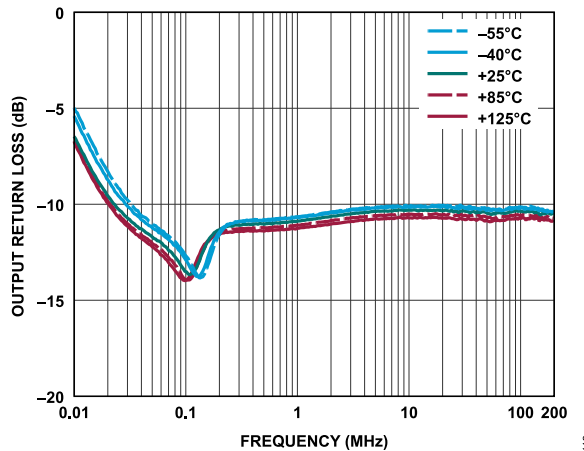


Figure 112. Output Return Loss vs. Frequency for Various Temperatures, 10 kHz to 200 MHz

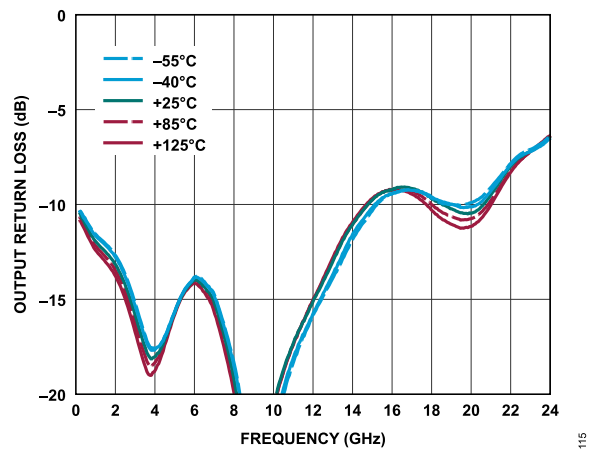


Figure 115. Output Return Loss vs. Frequency for Various Temperatures, 200 MHz to 24 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

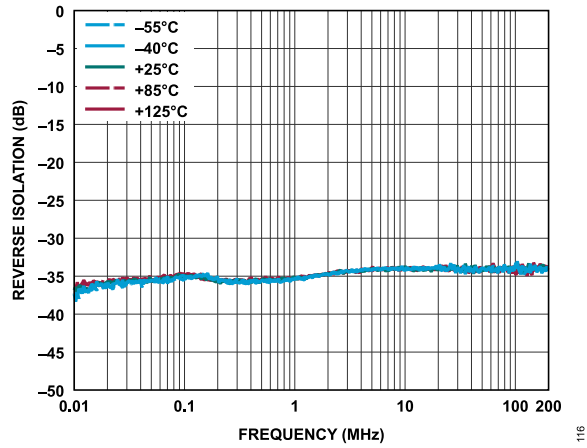


Figure 116. Reverse Isolation vs. Frequency for Various Temperatures, 10 kHz to 200 MHz

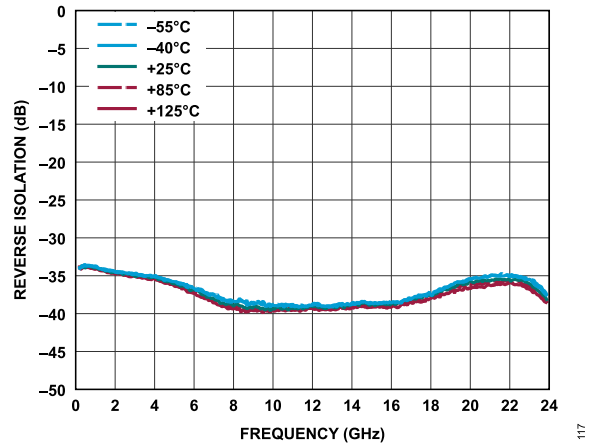


Figure 117. Reverse Isolation vs. Frequency for Various Temperatures, 200 MHz to 24 GHz

THEORY OF OPERATION

The ADL8101 is a wideband LNA that operates from 10 kHz to 22 GHz. A simplified block diagram is shown in [Figure 118](#).

The ADL8101 has DC-coupled, single-ended input and output ports with impedance that is nominally equal to 50 Ω over the specified frequency range. AC input and output coupling capacitors and a bias inductor are the only external matching components required. To adjust I_{DQ} , connect an external resistor between the RBIAS and VDDx pins. The RFOUT/VDD1 pin provides the drain current. However, the drain bias voltage can also be resistively biased by connecting the ACG/VDD2 pin to an external supply.

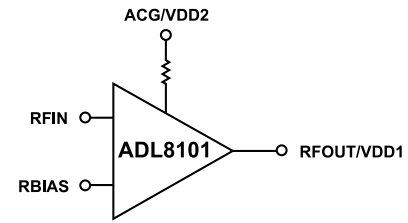


Figure 118. Simplified Schematic

118

APPLICATIONS INFORMATION

The basic connections for operating the ADL8101 from 10 MHz to 22 GHz are shown in Figure 121. AC-couple the input and output of the ADL8101 with appropriately sized capacitors (such as TDK Corporation Part Number C1005X7S1A105K050BC).

The bias conditions, $V_{DD} = 5\text{ V}$ and $I_{DQ} = 90\text{ mA}$, are the recommended operating point to achieve specified performance. The gain and return loss of this circuit are shown in Figure 119 and Figure 120 across frequencies. To set other bias conditions, adjust the R_{BIAS} value. Table 8 shows the recommended R_{BIAS} values and their associated I_{DQ} values.

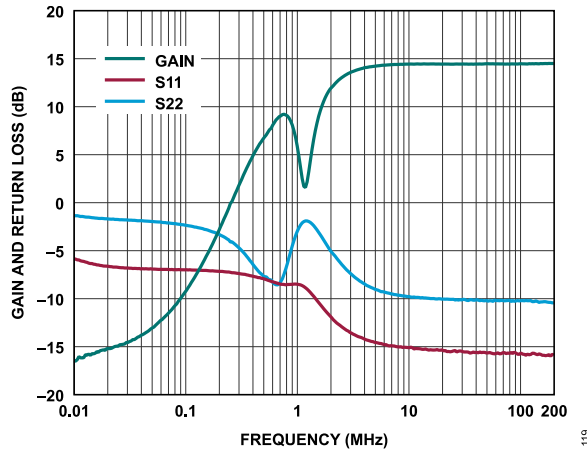


Figure 119. Gain and Return Loss vs. Frequency of 10 MHz to 22 GHz
Application Circuit, 10 kHz to 200 MHz,
 $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, $R_{BIAS} = 715\ \Omega$

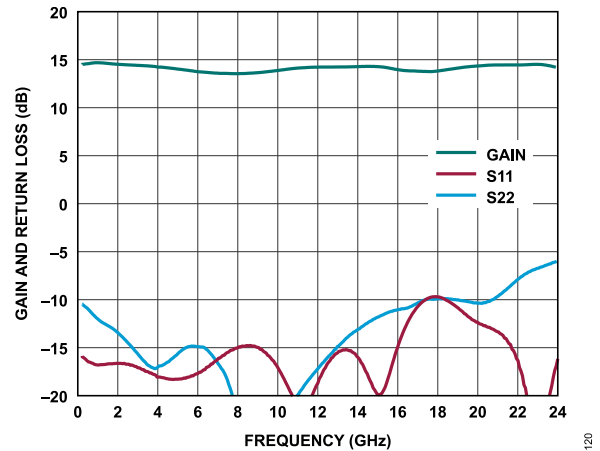


Figure 120. Gain and Return Loss vs. Frequency of 10 MHz to 22 GHz
Application Circuit, 200 MHz to 24 GHz,
 $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, $R_{BIAS} = 715\ \Omega$

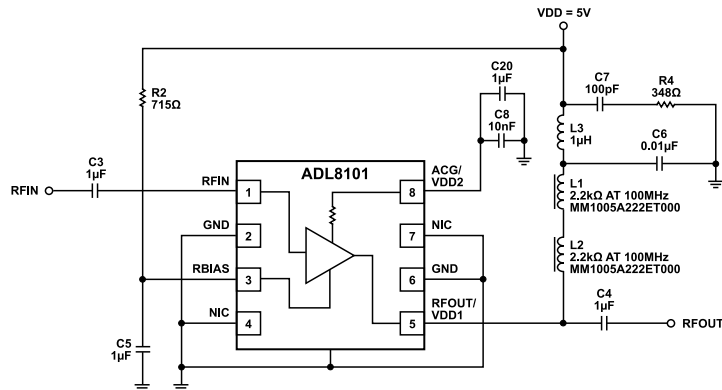


Figure 121. Typical Application Circuit for Operation from 10 MHz to 22 GHz

APPLICATIONS INFORMATION

RECOMMENDED BIAS SEQUENCING

The correct sequencing of the DC and RF power is required to safely operate the ADL8101. During power-up, apply V_{DD} before the RF power is applied to RFIN, and during power off, remove the RF power from RFIN before V_{DD} is powered off.

For more information on using the evaluation board, refer to the [EVAL-ADL8101](#) user guide.

**Table 8. Recommended Bias Resistor Values for Various I_{DQ} Values,
 $V_{DD} = 5 V$**

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
1920	50	47.8	2.2
1066	70	66	4
715	90	84.5	5.5
515	110	102.8	7.2
390	130	121	9

**Table 9. Recommended Bias Resistor Values for Various Supply Voltages,
 $I_{DQ} = 90 mA$**

R_{BIAS} (Ω)	V_{DD} (V)
256	3.0
473	4.0
715	5.0
968	6.0

APPLICATIONS INFORMATION

OPERATION FROM 10 KHZ TO 22 GHZ

Figure 124 shows the application circuit that was used to extend operation down to 10 kHz. Components, L3 = 680 μH and R4 = 300 Ω, support the low frequency operation. The gain and the return loss of this circuit are shown in Figure 122 and Figure 123.

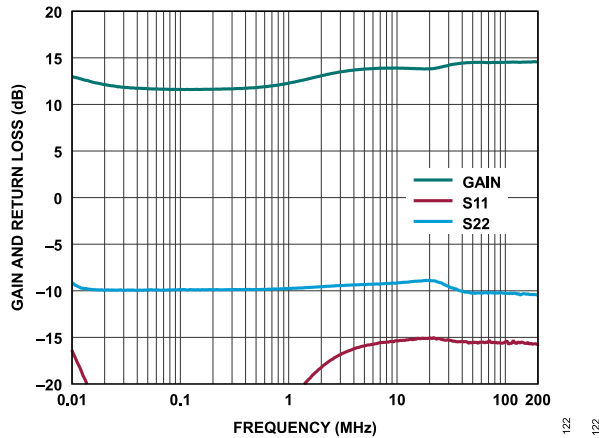


Figure 122. Gain and Return Loss vs. Frequency of 10 kHz to 22 GHz
Application Circuit, 10 kHz to 200 MHz,
 $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, $R_{BIAS} = 715\ \Omega$

Further adjustments can be made to the external components of the device to operate at even lower frequencies. Specifically, the bias tee and DC blocking capacitors can be modified because these components are the limiting factor causing the low frequency cutoff. These external components can be interchanged to support low frequency operation.

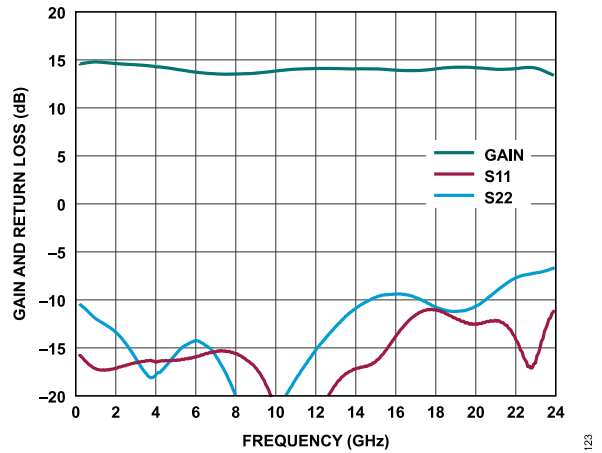


Figure 123. Gain and Return Loss vs. Frequency of 10 kHz to 22 GHz
Application Circuit, 200 MHz to 24 GHz,
 $V_{DD} = 5\text{ V}$, $I_{DQ} = 90\text{ mA}$, $R_{BIAS} = 715\ \Omega$

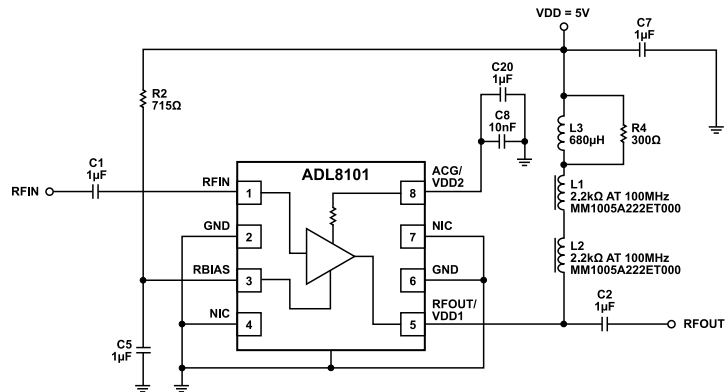


Figure 124. Typical Application Circuit for Operation from 10 kHz to 22 GHz

APPLICATIONS INFORMATION

PROVIDING DRAIN BIAS THROUGH THE ACG/VDD2 PIN

An alternative way to bias the ADL8101 is through the ACG/VDD2 pin (Pin 8), which is shown in [Figure 125](#). Because of the voltage drop across the internal bias resistor, a higher V_{DD} is required. If a $715\ \Omega$ bias resistor ($R2$) is used and connected to the 5 V power supply, which results in a total current of 90 mA, a V_{DD} of 8.5 V is recommended. $R2$ can also be connected to the V_{DD} of 8.5 V. In this case, to set I_{DQ} to 90 mA, use an $R2$ value of $1350\ \Omega$ on RBIAS.

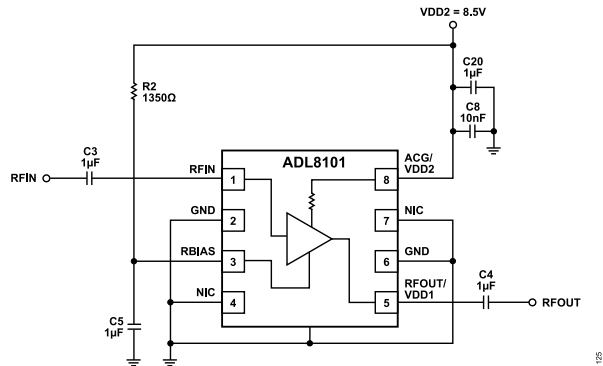


Figure 125. Providing Resistive Drain Bias Through the ACG/VDD2 Pin

APPLICATIONS INFORMATION

OVERDRIVE RECOVERY OPTIMIZATION

The overdrive recovery performance of the 10 MHz to 22 GHz circuit can be improved by adjusting the C1. Figure 78 is the overdrive recovery time performance comparison of the baseline ADL8101-EVALZ configuration vs. the optimized ADL8101-EVALZ. The input DC blocking capacitor is the major component for slowing down the recovery time. C1 = 100 pF is the selected value with the least effect on the recovery time performance. Figure 126 shows the gain and return loss of the modified optimized application circuit.

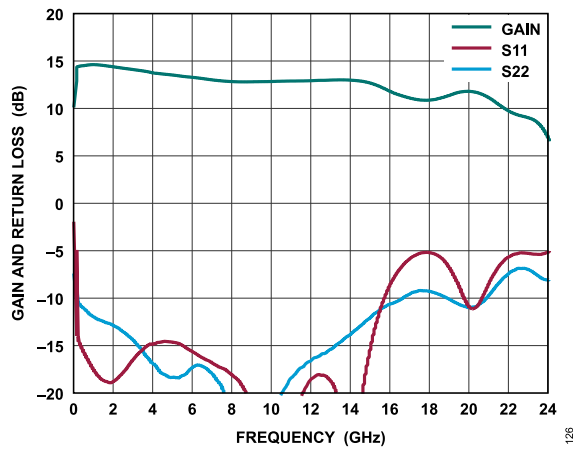


Figure 126. Gain and Return Loss vs. Frequency for EVAL-ADL8101 Overdrive Recovery Time Optimized Circuit, 10 MHz to 22 GHz, $V_{DD} = 5\text{ V}$, $R_{BIAS} = 715\ \Omega$

APPLICATIONS INFORMATION

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 127 shows a recommended power management circuit for the ADL8101. The LT8607 step-down regulator is used to step down a 12 V rail to 4.5 V that is then applied to the LT3042 low dropout (LDO) linear regulator to generate a low noise 3.3 V output. Even though the circuit shown in Figure 127 has an input voltage (V_{IN}) of 12 V, the input range to the LT8607 can be as high as 42 V.

The 4.5 V regulator output of the LT8607 is set by the R2 and R3 resistors, according to the following equation:

$$R2 = R3((VOUT/0.778 \text{ V}) - 1)$$

where VOUT is the output voltage.

The switching frequency (f_{SW}) is set to 2 MHz by the 18.2 k Ω resistor (R1) on the RT pin of the LT8607. The LT8607 data sheet provides a table of resistor values that can be used to select other switching frequencies ranging from 0.2 MHz to 2.200 MHz.

The output voltage of the LT3042 is set by the R4 resistor connected to the SET pin, according to the following equation:

$$VOUT = 100 \mu\text{A} \times R4$$

The resistors on the PGFB pins of the LT3042 are chosen to trigger the power-good (PG) signal when the output is just under 95% of the target voltage of 3.3 V. The output of the LT3042 has 1% initial

tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature, and adding resistors results in a bit more tolerance (5%). Therefore, putting 5% between the output and PGFB works well. In addition, the PG open-collector is pulled up to the 3.3 V output to give a convenient 0 V to 3.6 V voltage range. Table 10 provides the recommended resistor values for operation at 3.6 V to 3 V.

Table 10. Recommended Resistor Values for Operating at 3.6 V to 3 V

LDO VOUT (V)	R4 (k Ω)	R7 (k Ω)	R8 (k Ω)
3.6	36.5	332	30.1
3.3	33.1	301	30.1
3	30.1	267	30.1

The LT8607 can source a maximum current of 750 mA, and the LT3042 can source a maximum current of 200 mA. If the 5 V power supply voltage is being developed as a bus supply to serve another component, higher current devices can be used. The LT8608 and LT8609 step-down regulators can source a maximum current to 1.5 A and 3 A, respectively, and these devices are pin compatible with the LT8607. The LT3045 linear regulator, which is pin compatible with LT3042, can source a maximum current to 500 mA.

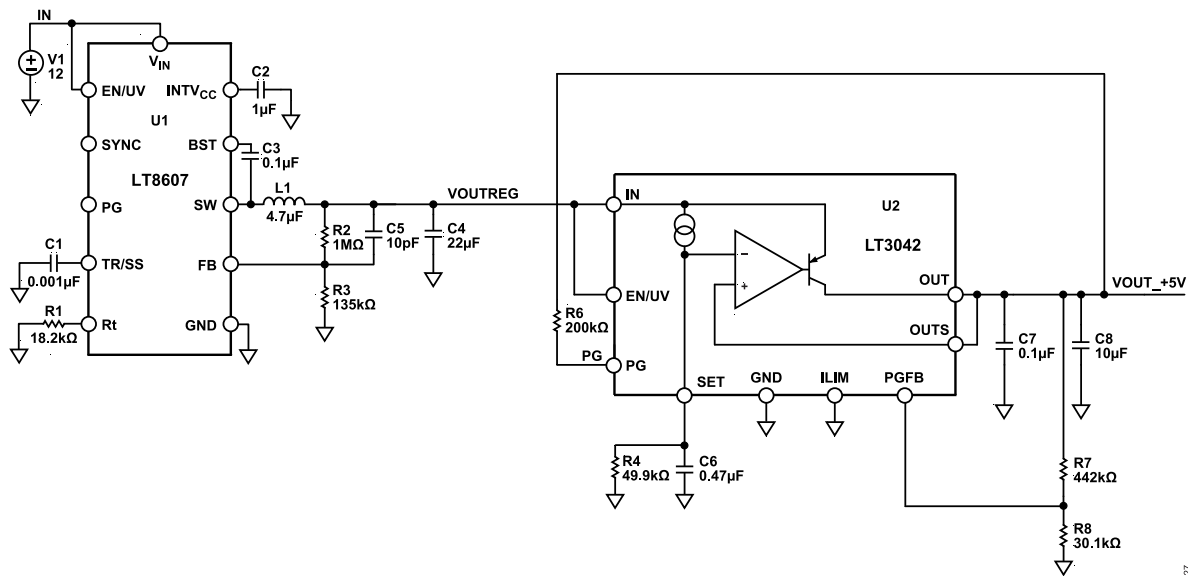
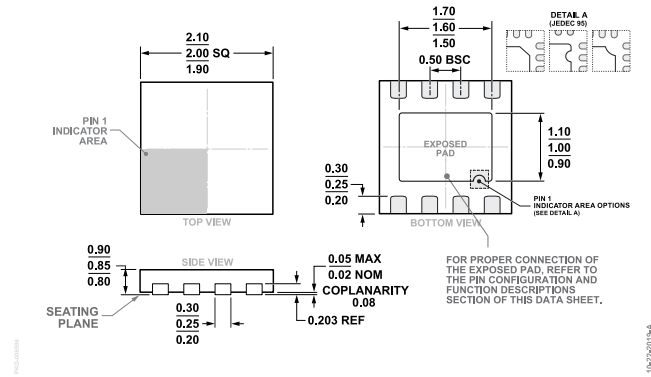


Figure 127. Recommended Power Management Circuit

OUTLINE DIMENSIONS



**Figure 128. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.85 mm Package Height
(CP-8-30)
Dimensions shown in millimeters**

ORDERING GUIDE

Model ^{1,2}	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8101ACPZN	-55°C to +125°C	8-lead LFCSP, 2 mm × 2 mm × 0.85 mm	Tape, 1	CP-8-30
ADL8101ACPZN-R7	-55°C to +125°C	8-lead LFCSP, 2 mm × 2 mm × 0.85 mm	Reel, 3000	CP-8-30

¹ Z = RoHS Compliant Part.

² The lead finish of the ADL8101ACPZN and the ADL8101ACPZN-R7 is nickel palladium gold.

EVALUATION BOARDS

Model ¹	Description
ADL8101-EVALZ	ADL8101 Evaluation Board for 10 MHz to 22 GHz
ADL8101-EVAL1Z	ADL8101 Evaluation Board for 10 kHz to 22 GHz

¹ Z = RoHS Compliant Part.