IOR HiRel
An Infineon Technologies Company

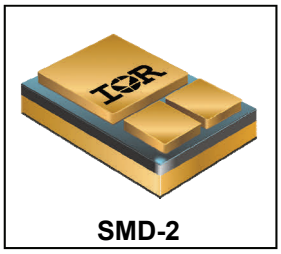
IRHSLNA57064

RADIATION HARDENED SYNCHRONOUS RECTIFIER SURFACE MOUNT (SMD-2)

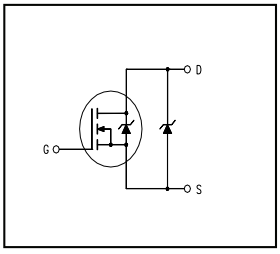
60V, N-CHANNEL

Product Summary

Part Number	Radiation Level	RDS(on)	Q_G
IRHSLNA57064	100 kRads(Si)	6.1mΩ	160nC
IRHSLNA53064	300 kRads(Si)	6.1mΩ	160nC
IRHSLNA54064	600 kRads(Si)	6.1mΩ	160nC
IRHSLNA58064	1000 kRads(Si)	6.1mΩ	160nC



SMD-2



Description

The SynchFet family of Co-Pack RAD-Hard MOSFETs and Schottky diodes offers the designer an innovative, board space saving solution for switching regulator and power management applications. RAD-Hard MOSFETs utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. Combining this technology with IR Hirel low forward drop Schottky rectifiers results in an extremely efficient device suitable for use in a wide variety of Military and Space applications.

Features

- Co-Pack N-channel RAD-Hard MOSFET and Schottky Diode
- Ideal for Synchronous Rectifiers in DC-DC Converters up to 75A Output
- Low Conduction Losses
- Low Switching Losses
- Low Vf Schottky Rectifier
- ESD Rating: Class 3B per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = 12V, T_C = 25°C	Continuous Drain or Source Current	75*	A
I_{D2} @ V_{GS} = 12V, T_C = 100°C	Continuous Drain or Source Current	75*	
I_{DM} @T_C = 25°C	Pulsed Drain Current ①	300	
P_D @T_C = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ④	370	mJ
I_{AR}	Avalanche Current ①	75	A
E_{AR}	Repetitive Avalanche Energy ①	25	mJ
I_F (AV) @ T_C = 25°C	Schottky and Body Diode Avg. Forward Current ③	75*	A
I_F (AV) @ T_C = 100°C	Schottky and Body Diode Avg. Forward Current ③	75*	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Package Mounting Surface Temp.	300 (for 5s)	
	Weight	3.3 (Typical)	g

* Current is limited by package

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	——	——	V	V_{GS} = 0V, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	6.1	mΩ	V_{GS} = 12V, I_D = 45A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
Gfs	Forward Transconductance	45	——	——	S	V_{DS} = 15V, I_D = 45A ④
I_{DSS}	Zero Gate Voltage Drain Current	——	——	90	µA	V_{DS} = 48V, V_{GS} = 0V
		——	——	50	mA	V_{DS} = 48V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	——	——	-100		V_{GS} = -20V
Q_G	Total Gate Charge	——	——	160	nC	I_D = 45A
Q_{GS}	Gate-to-Source Charge	——	——	55		V_{DS} = 30V
Q_{GD}	Gate-to-Drain ('Miller') Charge	——	——	65		V_{GS} = 12V
$t_{d(on)}$	Turn-On Delay Time	——	——	35	ns	V_{DD} = 30V
tr	Rise Time	——	——	125		I_D = 45A
$t_{d(off)}$	Turn-Off Delay Time	——	——	75		R_G = 2.35Ω
t_f	Fall Time	——	——	50		V_{GS} = 12V
Ls +L_D	Total Inductance	——	6.6	——	nH	Measured from center of Drain pad to center of Source pad

Schottky Diode and Body Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{SD}	Diode Forward Voltage	——	——	0.93	V	T_J=-55°C, I_S= 45A, V_{GS}=0V④
		——	——	0.9		T_J=25°C, I_S= 45A, V_{GS}=0V④
		——	——	0.82		T_J=125°C, I_S= 45A, V_{GS}=0V④
t_{rr}	Reverse Recovery Time	——	——	100	ns	T_J=25°C, I_F = 45A,V_{DD} ≤ 30V
Q_{rr}	Reverse Recovery Charge	——	——	210	nC	di/dt = 100A/µs ④
L_S +L_D	Total Inductance	——	7.95	——	nH	Measured from center of drain pad to center of source pad (for Schottky only)
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case (MOSFET)	——	——	0.5	°C/W
$R_{\theta JC}$	Junction-to--Case (Schottky)	——	——	0.7	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

③ 50% Duty Cycle, Rectangular

④ V_{DD} = 25V, starting T_J = 25°C, L = 0.13mH, Peak I_L = 75A, V_{GS} = 12V

⑤ Total Dose Irradiation with V_{GS} Bias. 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑥ Total Dose Irradiation with V_{DS} Bias. 48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑦ Specified Radiation Characteristics are for Radiation Hardened MOSFET die only.

Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥⑦

Symbol	Parameter	Up to 600 kRads (Si)[1]		1000 kRads (Si)[2]		Units	Test Conditions
		Min.	Max.	Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	——	60	——	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	1.5	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	——	100	——	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	——	-100	——	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	——	10	——	25	µA	V_{DS} = 48V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	——	6.1	——	7.1	mΩ	V_{GS} = 12V, I_D = 45A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (SMD-2)	——	6.1	——	7.1	mΩ	V_{GS} = 12V, I_D = 45A
V_{SD}	Diode Forward Voltage ④	——	1.3	——	1.3	V	V_{GS} = 0V, I_S = 45A

1. Part numbers IRHSLNA57064, IRHSLNA53064 and IRHLSNA54064
2. Part numbers IRHSLNA58064

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	VDS (V)				
			@ VGS = 0V	@ VGS=-5V	@ VGS=-10V	@ VGS =-15V	@ VGS=-20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	60	60	60	60	30
61 ± 5%	330 ± 7.5%	31 ± 10%	46	46	35	25	15
84 ± 5%	350 ± 10%	28 ± 7.5%	35	30	25	20	14

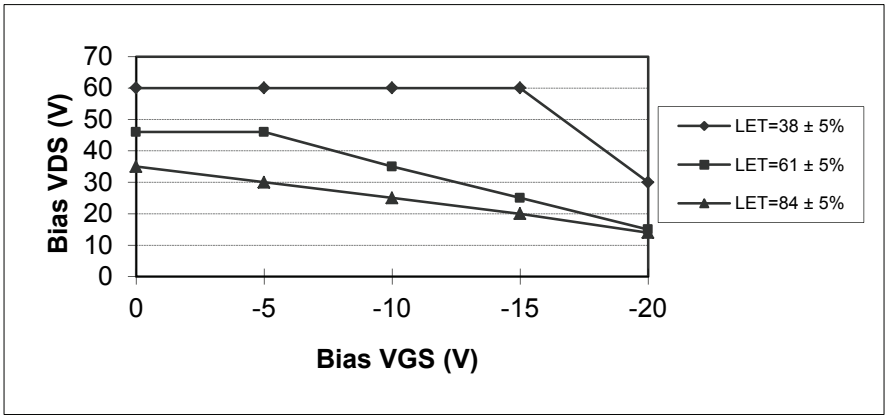


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

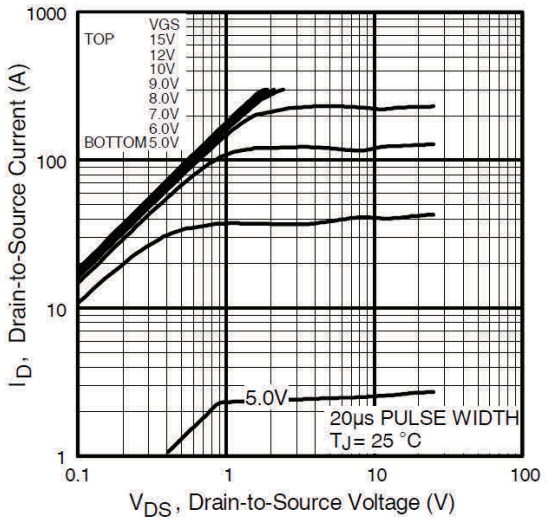


Fig 1. Typical Output Characteristics

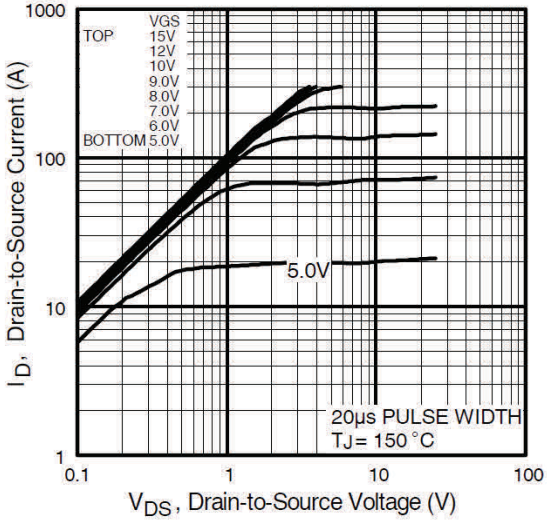


Fig 2. Typical Output Characteristics

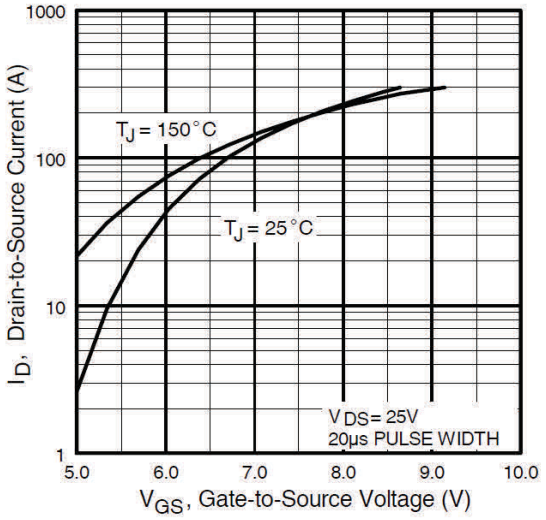


Fig 3. Typical Transfer Characteristics

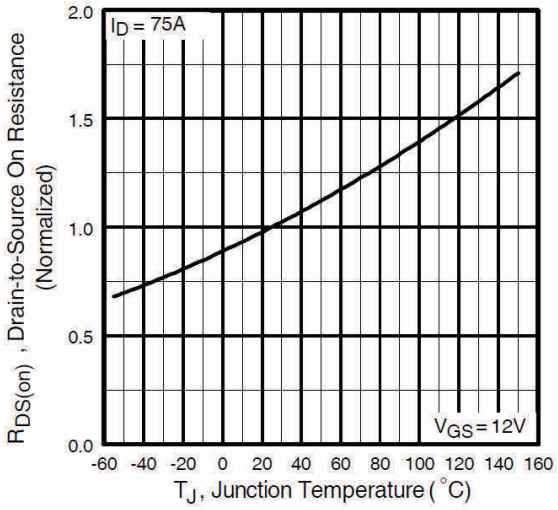


Fig 4. Normalized On-Resistance Vs. Temperature

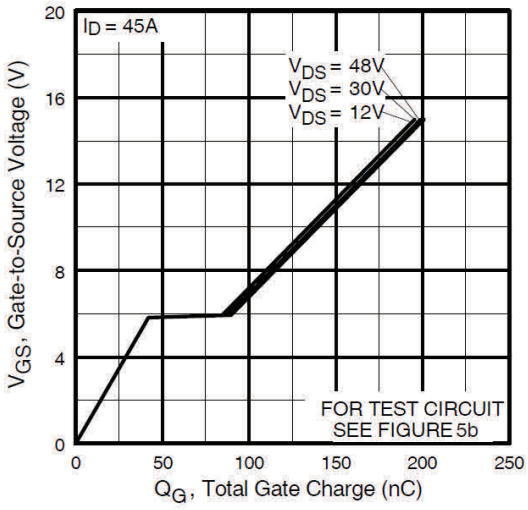


Fig 5. Typical Gate Charge Vs. Gate-to-Source Voltage

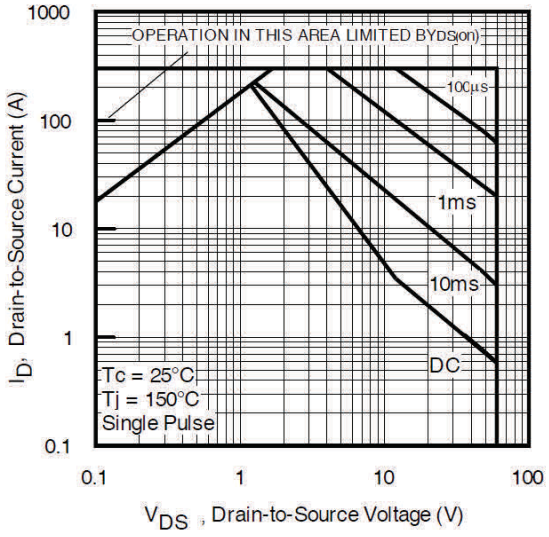


Fig 6. Maximum Safe Operating Area

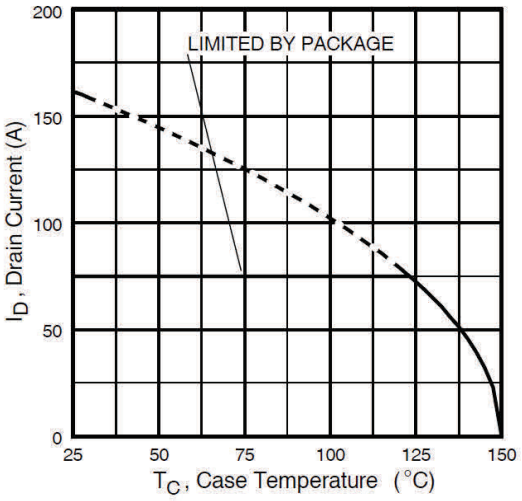


Fig 7. Maximum Drain Current Vs. Case Temperature

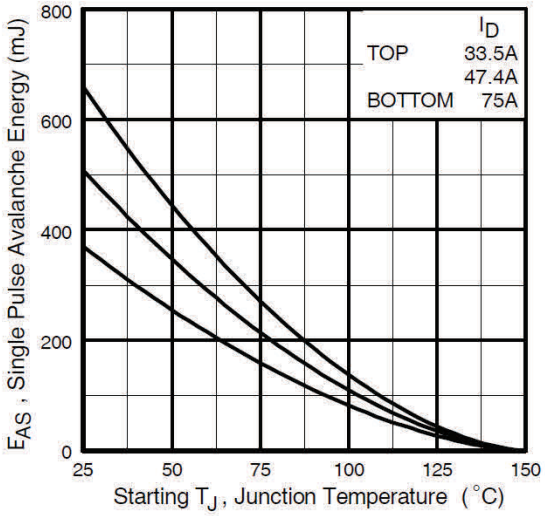


Fig 8. Maximum Avalanche Energy Vs. Drain Current

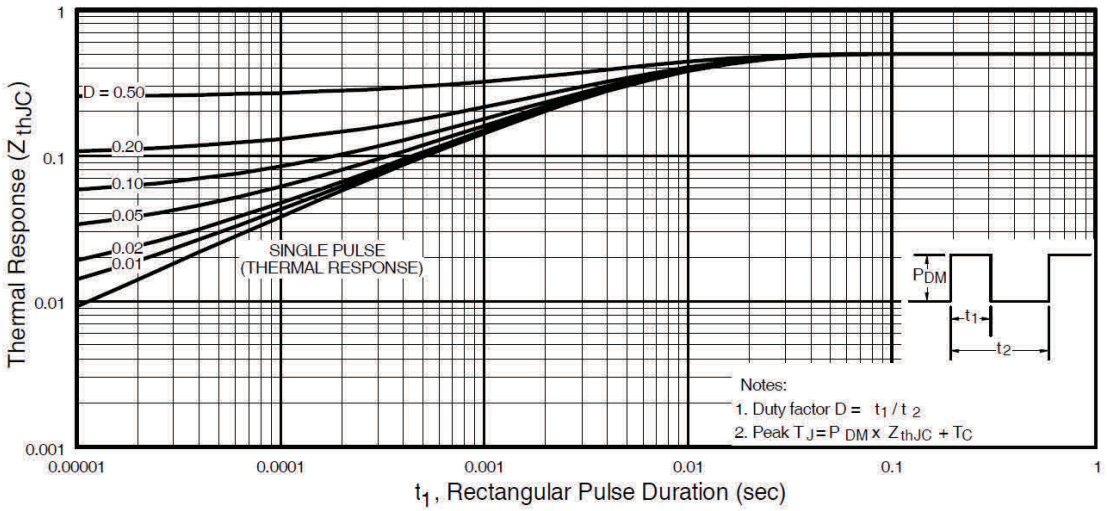


Fig 9. Maximum Effective Transient Thermal Impedance, Junction-to-Case, MOSFET

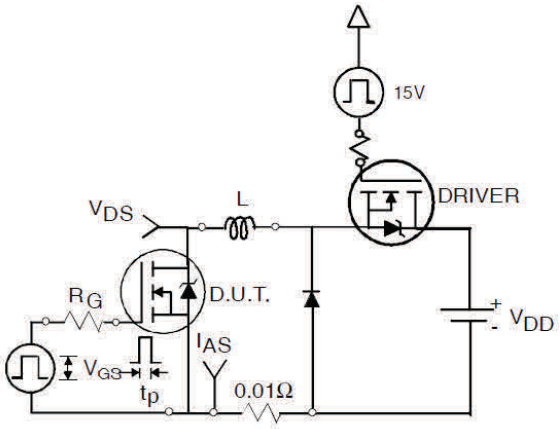


Fig 10a. Unclamped Inductive Test Circuit

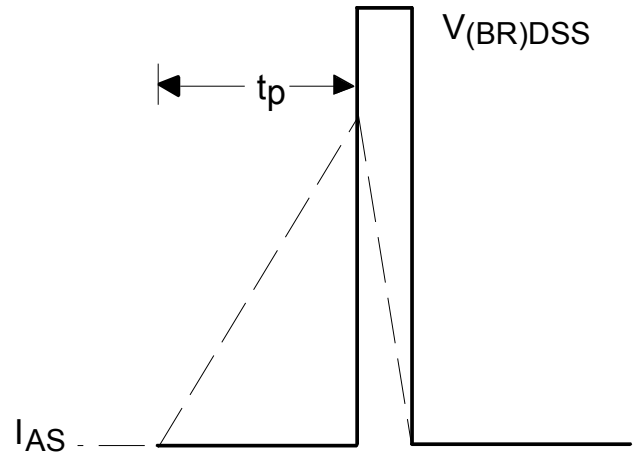


Fig 10b. Unclamped Inductive Waveforms

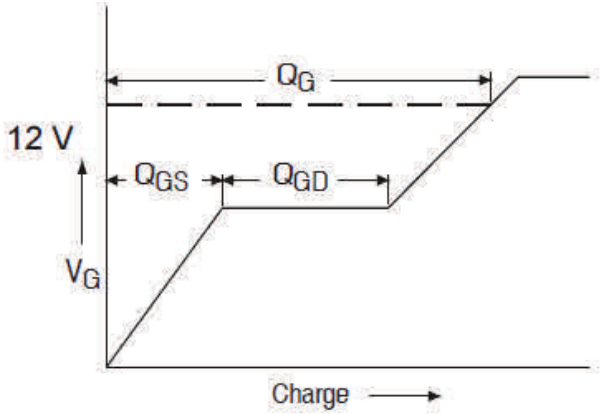


Fig 11a. Gate Charge Waveform

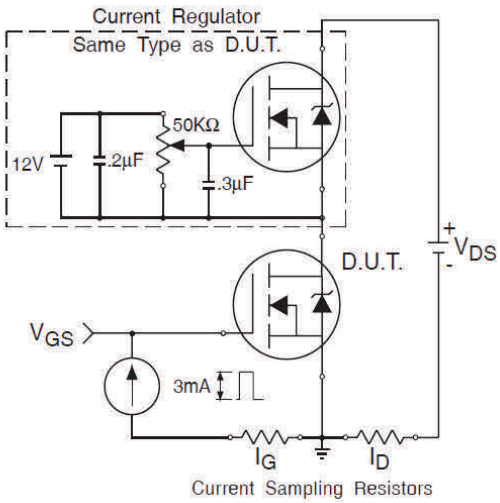


Fig 11b. Gate Charge Test Circuit

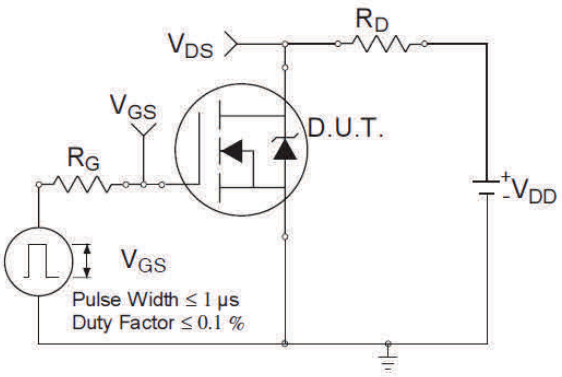


Fig 12a. Switching Time Test Circuit

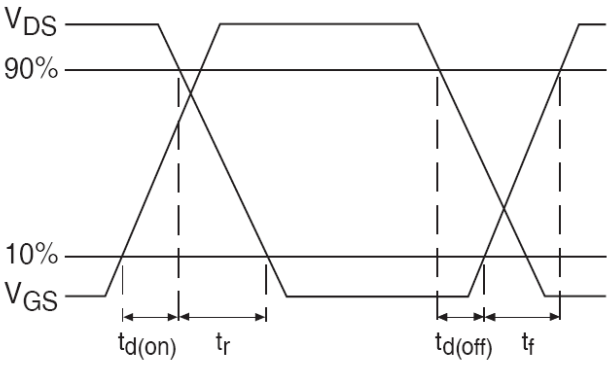


Fig 12b. Switching Time Waveforms

MOSFET Body Diode & Schottky Diode Characteristics

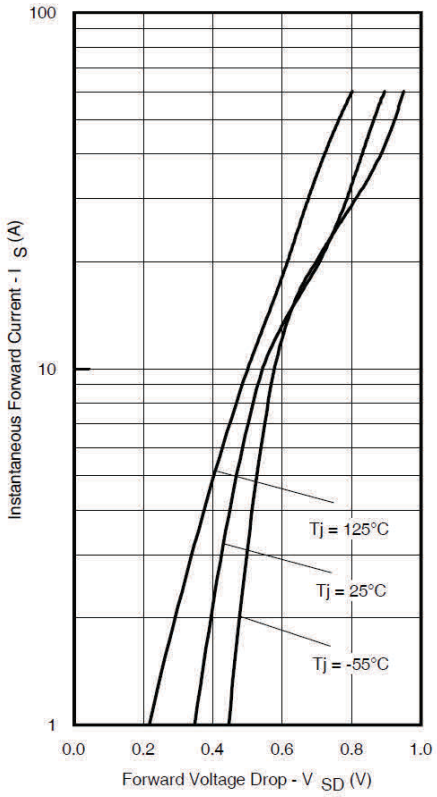


Fig 13. Typical Forward Voltage Drop Characterstics

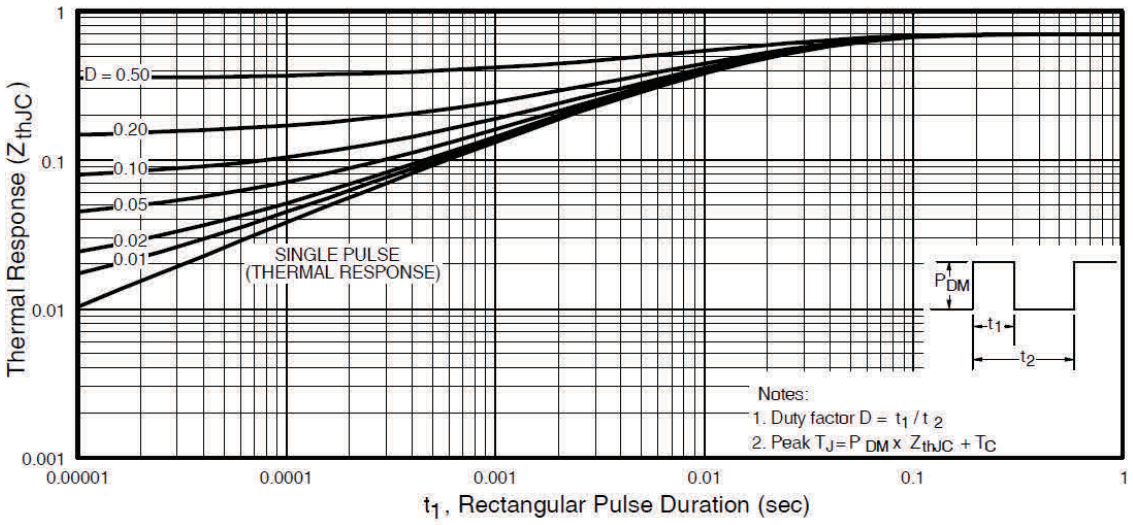
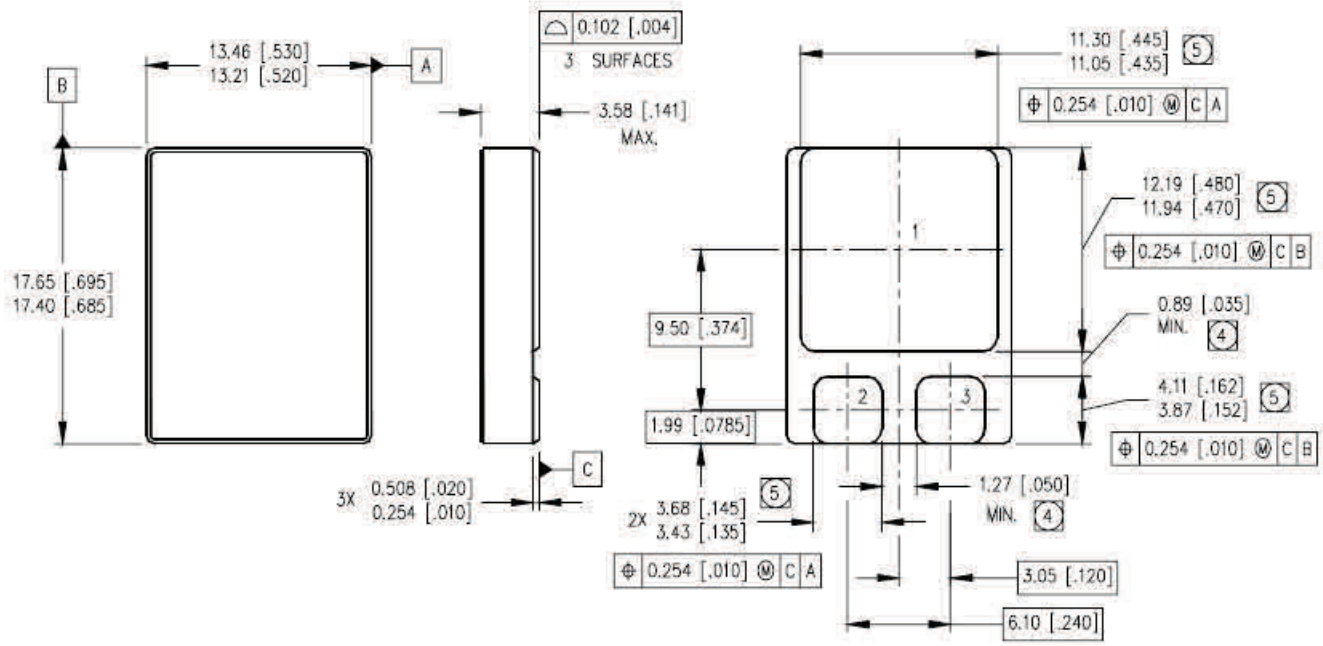


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case , Schottky

Case Outline and Dimensions — SMD-2



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. (4) DIMENSION INCLUDES METALLIZATION FLASH.
5. (5) DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

1 = DRAIN
2 = GATE
3 = SOURCE

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